Superjunction MOSFET

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ABSTRACT

600 V-class superjunction (SJ) MOSFETs (package : TO-220) with a maximum on-resistance of 0.16 Ω have been fabricated by using multi-epitaxial growth technology which has an excellent capability for controlling the doping concentration. By optimizing the doping concentration in the SJ structure, the fabricated SJ-MOSFET achieves an approximate 70% reduction in specific on-resistance compared to that of a conventional MOSFET "SuperFAP-E^3." This is the industry's highest level of specific on-resistance, and its value exceeds the theoretical limit for conventional MOSFETs. The avalanche withstand capability of the fabricated SJ-MOSFET has been also improved over the rated current by optimizing the doping profile of the SJ structure in the depth direction and the thickness and resistivity of the n-buffer layer.

1. Introduction

In recent years, as concern for protecting the global environmental has heightened, in the IT (information technology) sector, green IT has been attracting attention as a way to achieve power savings. In order to reduce the power loss of IT equipment, the power converters used with the IT equipment must be made more efficient. Consequently there is strong demand for low-loss power MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors). The power MOSFETs used in power converters operate as switching devices and their associated dissipation loss consists of conduction loss while the power MOSFET is ON, and switching loss when the power MOSFET turns on and turns off. Generally, the conduction loss is dominant in applications having a low switching frequency, and the switching loss is dominant in applications having a high switching frequency. The on-resistance normalized to a unit area ($R_{on}\cdot A$) is used as a figure of merit for the conduction loss, and the gate-to-drain charge normalized to the on-resistance ($R_{on}\cdot Q_{GD}$) is used as a figure of merit for the switching loss. Thus, in order to reduce the dissipation loss of a power MOSFET, minimization of these figures of merit is strongly requested.

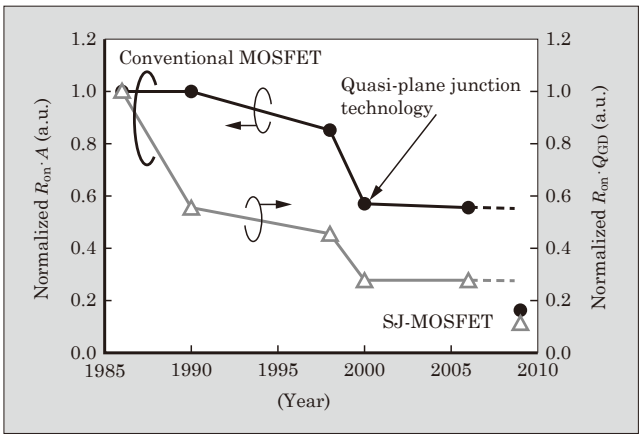
However, the breakdown voltage and $R_{on}\cdot A$ are associated with a theoretical limit that is determined by the material (in the case of silicon, this theoretical limit is known as the silicon limit), and it is not thought to be possible to obtain a $R_{on}\cdot A$ value that exceeds this theoretical limit. The super junction (SJ) structure is an innovative breakthrough that overcomes this limitation, and is attracting attention due to its ability to realize dramatically lower $R_{on}\cdot A$[1][2].

This paper describes the fabrication method and characteristics of Fuji Electric's newly developed 600 V-class SJ-MOSFET that realizes the lowest on-resistance in the industry and a high level of inductive load avalanche withstand capability.

2. Technical Trends of Power MOSFETs

Figure 1 shows the trends of $R_{on}\cdot A$ and $R_{on}\cdot Q_{GD}$ for 600 V-class power MOSFETs. As described above, a theoretical limit exists for the $R_{on}\cdot A$ of the power MOSFET, and therefore development efforts until now have focused on how to make the $R_{on}\cdot A$ approach the silicon limit as closely as possible. In order to reduce the $R_{on}\cdot A$, the drift resistance, which forms the silicon limit, was reduced and other resistance components were also reduced. The latter entails reducing the channel resistance and JFET (Junction Field-Effect Transistor) resistance by improving the cell density

Fig.1 Power MOSFET $R_{on}\cdot A$ and $R_{on}\cdot Q_{GD}$ trends



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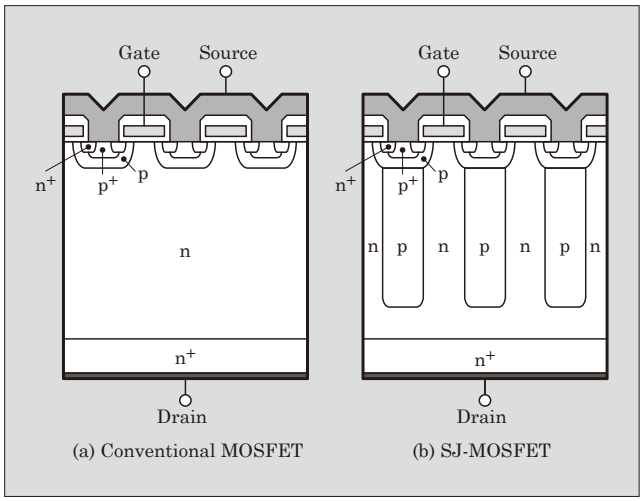
of the surface MOSFET area and optimizing the cell structure, and the former entails reducing the drift resistance by optimizing the resistivity and thickness of the drift layer that ensure the inductive load avalanche withstand capability and the breakdown voltage. With a structure that uses a p-well region to ensure the inductive load avalanche withstand capability, there is a limit to extent with which the drift resistance can be reduced, but the application of quasi-plane junction technology enables this limit to be lowered[3]. With quasi-plane junction technology, instead of using a p-well structure, the drift resistance is reduced by narrowing the distance between p-base regions without increasing the JFET resistance, and by optimizing the p-base shape, an inductive load avalanche withstand capability equivalent to that of a p-well structure is guaranteed. By applying quasi-plane junction technology, the $R_{on} \cdot A$ of a conventional MOSFET has been improved to 110% of the silicon limit, and the $R_{on} \cdot Q_{GD}$ has also been improved significantly with the reduction in $R_{on} \cdot A$ and the narrower distance between p-base regions. Fuji Electric has applied this quasi-plane junction technology to commercialize the "SuperFAP-G Series" which is an easy-to-use successor of the "SuperFAP-E^3 Series[4]."

Recently, the SJ-MOSFET, which breaks through the silicon limit, has been attracting attention. As shown in Fig. 2, the SJ-MOSFET replaces the p-type and n-type regions in the drift layer of a conventional MOSFET with alternating regions of p-pillars and n-pillars, and because the impurity concentration of the n-type regions can be increased, the $R_{on} \cdot A$ can be reduced dramatically. Moreover, since the $R_{on} \cdot A$ can be reduced, the active area can be made smaller for the same on-resistance, thereby enabling the $R_{on} \cdot Q_{GD}$ to be reduced as well.

Fig.2 Structure of conventional MOSFET and SJ-MOSFET

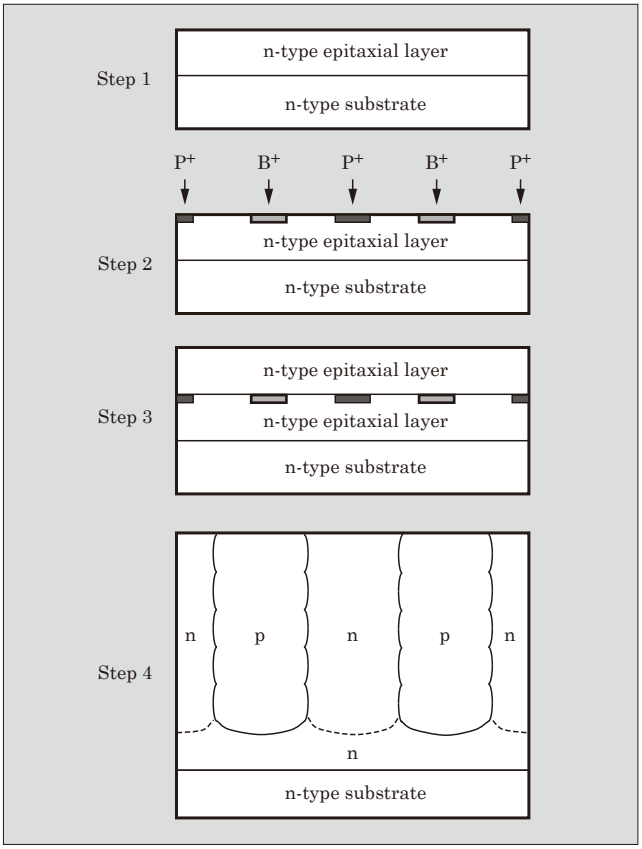


3. SJ-MOSFET Development

3.1 Multi-epitaxial growth technology

The SJ structure enables a dramatically lower value of $R_{on} \cdot A$, but because it is a charge compensation structure, it has the disadvantage of being unable to maintain its breakdown voltage unless a charge balance can be maintained between n-type and p-type regions. If the charge balance collapses, the breakdown voltage drops significantly and the rated voltage will not be maintainable. When fabricating an SJ-MOSFET, the impurity concentrations of the n-type and p-type regions must be controlled precisely. To reduce deviation of the breakdown voltage, the impurity concentration in the depth direction of the p-type region must be distributed. Therefore, the SJ structure is fabricated with a method of multi-epitaxial growth in which the processes of introducing impurities into a certain area by ion implantation, which has excellent impurity concentration control performance, and epitaxial growth are performed repeatedly[5]. Figure 3 shows the process flow of SJ structure fabrication by the multi-epitaxial growth method. First, an n-type layer having a low impurity concentration is grown epitaxially on an n-type substrate with consideration given to the thickness of the buffer layer (step 1). Next after completion of the fabrication of that layer, phosphorous (P) and boron (B) ions are injected into regions

Fig.3 SJ structure fabrication process flow using multi-epitaxial growth method



that will become n-type and p-type regions (step 2), and then an n-type layer having a low impurity concentration is grown epitaxially (step 3). Because the impurity concentrations in the fabricated n-type and p-type regions are determined by the dimensions of the resist for ion injection and by the accuracy of the ion injection itself, the impurity concentrations are easy to control. Steps 2 and 3 are repeated until a certain drift layer thickness is achieved, and then lastly, thermal diffusion is used to fabricate consecutive n-type and p-type regions. Thereafter, an ordinary DMOSFET (Double Diffused MOSFET) process is used to fabricate a DMOSFET on the surface of the SJ structure and create the SJ-MOSFET. Figure 4 shows an SCM (scanning capacitance microscopy) image of a cross-section of an SJ-MOSFET fabricated by the multi-epitaxial growth method. From the figure, it can be verified that an SJ structure, connected to both the p-type and n-type regions in the depth direction, has been fabricated.

Fig.4 SCM image of SJ-MOSFET cross-section

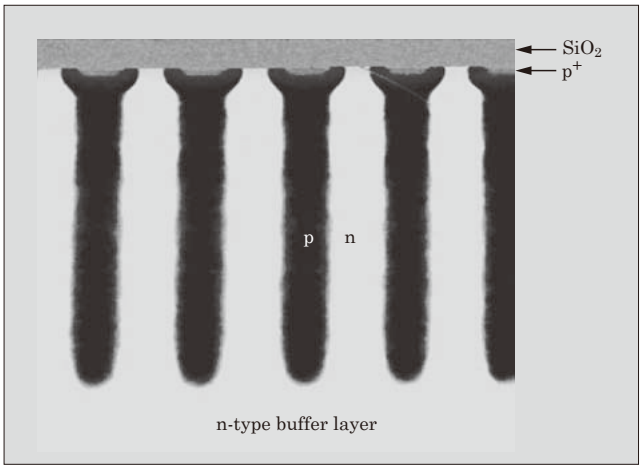
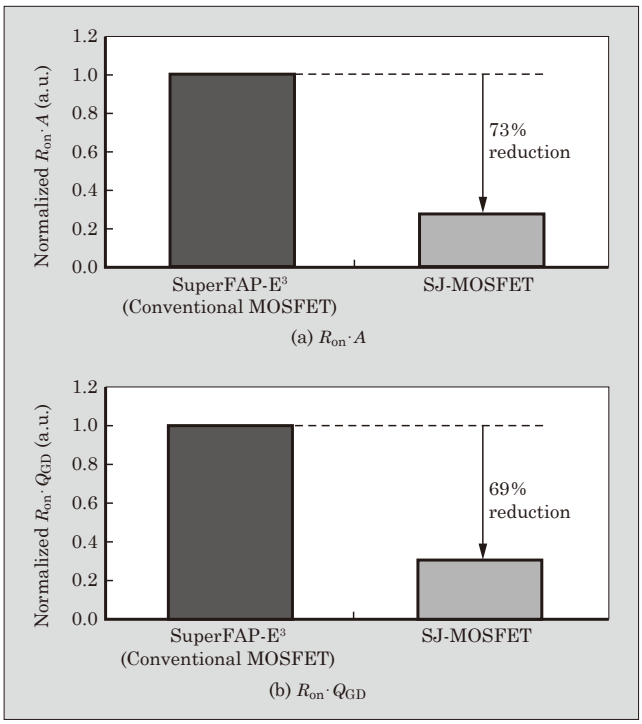


Fig.5 Comparison of figures of merit for conventional MOSFET and SJ-MOSFET



3.2 Improvement of R_{on}·A

Using the multi-epitaxial growth method, an SJ-MOSFET rated at 600 V and 0.16 Ω was developed. As shown in Fig. 5(a), the R_{on}·A of the developed SJ-MOSFET is approximately 73% lower than that of the SuperFAP-E^3, which is a conventional MOSFET. This is the industry's lowest level of R_{on}·A. A comparison of R_{on}·Q_{GD} is shown in Fig. 5(b). The R_{on}·Q_{GD} of the SJ-MOSFET is also approximately 69% lower than that of the SuperFAP-E^3. Moreover, the surface MOSFET structure of the SJ-MOSFET is based on the same concept as the SuperFAP-E^3 and inherits its ease-of-use. Figure 6 shows the output characteristics of the SJ-MOSFET for $V_{GS(th)}$=3.0 V.

Fig.6 Output characteristics of SJ-MOSFET

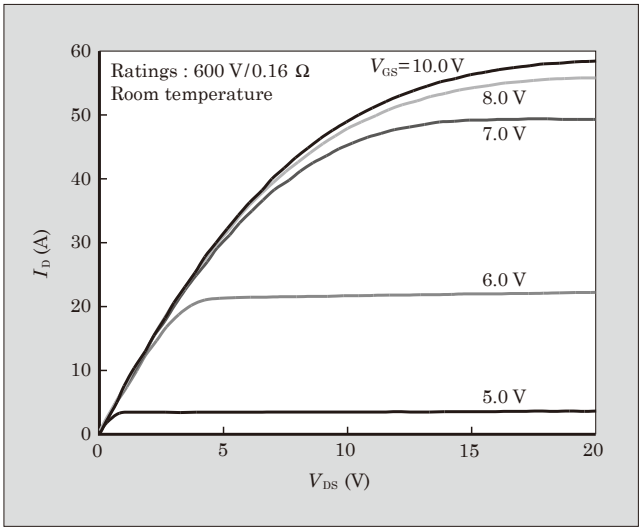


Fig.7 Inductive load avalanche waveform of SJ-MOSFET

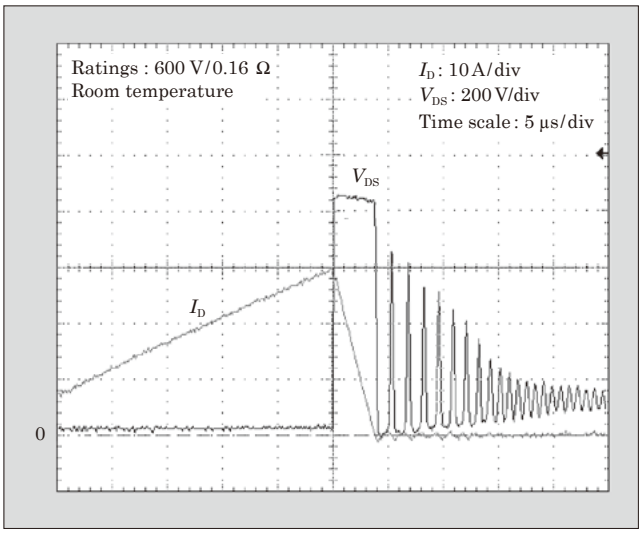


Fig.8 Power supply circuit for application evaluation

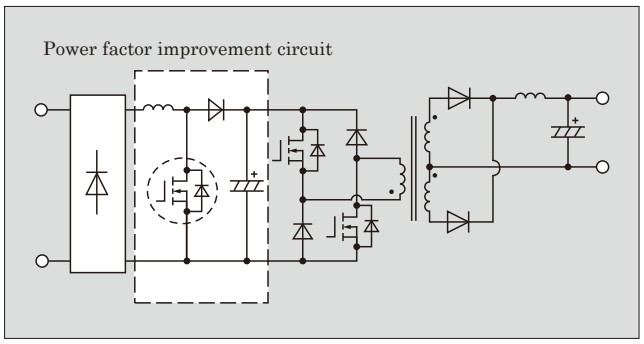
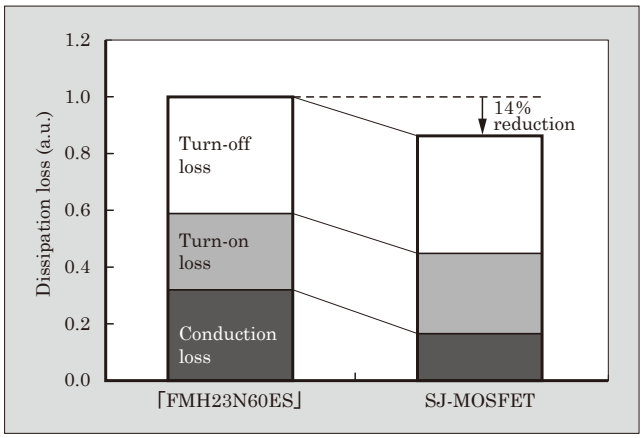


Fig.9 Comparison of power MOSFET dissipation loss (AC100 V input/400 W output)



3.3 Improved inductive load avalanche withstand capability

It has been noted that the inductive load avalanche withstand current of an SJ-MOSFET is less than that of a conventional MOSFET. As a result of an optimized impurity concentration profile and n-type buffer layer in the depth direction of the SJ structure, the newly developed SJ-MOSFET guarantees an inductive load avalanche withstand capability of 150 A/cm^2 even under a balanced charge condition. Figure 7 shows a typical inductive load avalanche waveform of an SJ-MOSFET.

4. Application Results

An SJ-MOSFET (rated at 600 V/0.16 Ω) fabricated with the multi-epitaxial growth method and assembled in a TO-220 package was installed in the power factor improvement circuit (Fig. 8) of a 400 W-class ATX power supply (server power supply that conforms to the ATX standard), and the loss and temperature rise were evaluated. Figure 9 compares the power MOSFET area loss for an SJ-MOSFET and for the FMH23N60ES (rated at 600 V and 0.16 Ω), which has the lowest on-resistance among SuperFAP-E^3 series products and is housed in a TO-3P package. Compared to the conventional FMH23N60ES MOSFET, the SJ-MOSFET realizes 16% lower conduction loss and an approximately 14% reduction in total power loss. Moreover, the temperature rise has been confirmed to be approximately 5 °C lower, and an approximate 0.5% improvement in the total power conversion efficiency has also been verified. Although differences exist between the TO-220 and TO-3P packages, simple replacement with an SJ-MOSFET can expect to yield a lower dissipation loss and improved efficiency.

5. Postscript

An SJ-MOSFET (in a TO-220 package) that is fabricated by multi-epitaxial growth technology and rated at 600 V and 0.16 Ω has been developed. The SJ-MOSFET features an optimized impurity concentration in the SJ structure and an optimized n-type buffer layer to achieve the industry's lowest level of low $R_{on}\cdot A$, and a high inductive load avalanche withstand capability. In the future, Fuji Electric intends to develop a product lineup of low-loss SJ-MOSFETs and to contribute to efforts for protecting the global environment.

References

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