Low On-Resistance Trench Lateral Power MOS Technology

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1. Introduction

Market demands for smaller sized, lighter weight, lower power consuming and higher efficiency portable electronic devices and communicative devices have propelled power ICs (integrated circuits) to become key components.

Fuji Electric has developed high breakdown voltage and low on-resistance power ICs, which drive DC-DC converters for portable electronic devices and plasma display panel drivers (PDPs).

Lateral power MOSFETs are generally used as switching devices and are integrated into power ICs. Required breakdown voltages of MOSFET devices range from 10 to 60 V for portable electronic devices and approximately 100 V for PDPs.

Fuji Electric has used a trench technology and has successfully improved the packing density of the MOSFET devices, achieving a very low on-resistance while keeping the breakdown voltage high.

Conventional Lateral Power MOSFET Technology with Low On-Resistance

Fuji Electric has developed technology for power ICs which integrates the 60 V-class planar-type LD-MOS (lateral double diffused MOS) devices illustrated in Fig. 1, and has applied these devices to ICs for power supplies in portable appliances⁽¹⁾. In the conventional planar-type LDMOS, the n⁻ drain with a high resistance is formed horizontally to release an electric field during the blocking mode. The n⁻ drain limits device packing density and restricts the reduction of on-resistance. In order to solve the problem, lateral MOSFET devices using trench technologies have been proposed. Nakagawa et al. fabricated trenches in the channel region to increase channel density⁽²⁾. Zitouni reduced device pitch by forming trenches in the n⁻ drain region⁽³⁾. However, the n⁻ drain is fabricated on the surface of the device in the above studies, and the packing density is limited. On the other hand, Fuji Electric proposed a trench lateral power MOSFET with a trench bottom drain contact (TLPM/D), where the channel and the n⁻ drain are

Fig.1 Planar-type LDMOS(1)



formed along the sidewall of the trench, reducing the device pitch to improve on-resistance⁽⁴⁾. However, the TLPM/D has a relatively high gate-to-drain capacitance between the plugged polysilicon drain and the gate ($C_{\rm gd2}$), which in addition to the capacitance between the gate and the n⁻ drain region ($C_{\rm gd1}$) as shown in Fig. 2, negatively effects switching performance of the device⁽⁴⁾.

3. Device Structure and Process Flow of TLPM/S

3.1 Device structure of TLPM/S

In order to improve the on-resistance and the switching performance, we proposed a Trench Lateral Power MOS device with a trench bottom source contact (TLPM/S)⁽⁵⁾. The cross-sectional view of the TLPM/S device is shown in Fig. 3. The TLPM/S device has an extended trench region at the lower part of the device. Since the source electrode is located at the bottom of the trench, the Miller capacitance of the device equals the gate-to-drain capacitance between the gate and the n⁻ drain region ($C_{\rm gd1}$), and is smaller than that of the TLPM/D device ($C_{\rm gd1} + C_{\rm gd2}$), resulting in faster switching speeds.

3.2 Process flow of TLPM/S

Process flow of the TLPM/S device fabrication is shown in Figs. 4(a) to 4(f). An n⁻ well region is formed on the p⁻ type silicon substrate and thick oxide is deposited on the n⁻ well region. Then a trench is etched using the mask oxide. Thereafter, the p⁻ body and n^- drain regions are formed on the sidewalls of the trench using tilted ion implantations as shown in Fig. 4(a). Next, the thick oxide is deposited on the surface of the substrate as shown in Fig. 4(b). Then, the oxide is etched back by using anisotropic etching and the trench is expanded at its bottom. In this step, the oxide is left on the sidewall of the trench as well as on the surface of the silicon substrate as shown in Fig. 4(c). Thereafter, the gate oxide is deposited on the





sidewall and at the bottom of the second trench, and the gate electrode is then formed by the deposition and anisotropic etching of polysilicon. The gate electrode and the thick oxide are used as masks to form the p base and n^+ source regions as shown in Fig. 4(d). Following this step, an insulating layer is deposited as shown in Fig. 4(e). Finally, a source contact at the bottom of the second trench is formed, followed by deposition of polysilicon on the inside surface of the





Fig.4 Fabrication process for TLPM/S



trench. Then surface leveling, contact formation and electrode definition are carried out as shown in Fig. 4(f).

In this process, the gate and source polysilicon electrodes are formed along the sidewall of the trench using a method of self-alignment and hence cell pitch is reduced.

4. Simulation Results

4.1 DC characteristics

The simulated specific on-resistance and breakdown voltage of the TLPM/S device as a function of the n^- drain dose are shown in Figs. 5(a) and (b), respectively. The on-resistance decreases monotonously with increasing n^- drain dose. This is because the resistance of the n^- drain region which dominates the total on-resistance is decreased due to the higher donor concentration in the n^- drain region. The breakdown voltage also decreases monotonously with increasing $n^$ drain dose because the expansion of the depletion layer is limited due to the higher donor concentration.

Distribution of the current density in the on-state for the TLPM/S device is shown in Fig. 6(a). In the onstate, the current flows from the drain to source along the sidewall of the trench as shown in Fig. 6(a). The distribution of the potential in the off-state for a

Fig.5 Simulated specific on-resistance and breakdown voltage for TLPM/S



TLPM/S device with a breakdown voltage of 73 V is shown in Fig. 6(b). In the off-state, the depletion layer spreads from the n^- drain region to the p^- silicon substrate. Due to the p base around the n^+ source region, punch-through breakdown is prevented.

4.2 Switching characteristics

Gate charge transfer characteristics of the TLPM/ S, the TLPM/D, and the planar-type LDMOS⁽¹⁾ devices are shown in Fig. 7, where the concentration of the channel and the thickness of the gate oxide are chosen so that the threshold voltages of the devices are equal to 1.0 V. Since the gate-to-drain capacitance of the TLPM/S device is lower than that of the TLPM/D, the amount of gate charge needed for a gate voltage of 5 V is smaller for the TLPM/S device than for the TLPM/D as is shown in Fig. 7. The amount of the gate charge for a gate voltage of 5 V in the case of the TLPM/S device is also smaller than that of the planar-type LDMOS because the input capacitance of the TLPM/S device is lower than that of the planar-type LDMOS.

Fig.6 Analysis of on- and off-states for TLPM/S



Fig.7 Simulated gate charge transfer characteristics



Fig.8 TEM micrograph of cross section of TLPM/S



5. Experimental Results

A TEM micrograph of the cross section of the fabricated TLPM/S device is shown in Fig. 8. The width of the first trench is $5.0 \,\mu\text{m}$. The depths of the first and second trenches are $4.0 \,\mu\text{m}$ and $1.2 \,\mu\text{m}$, respectively. The thick oxide along the first trench, the gate oxide along the second trench, and the source polysilicon which is used as a plug are observed.

The measured specific on-resistance and the breakdown voltage for the TLPM/S device as a function of the n⁻ drain dose are shown in Fig. 9(a) and (b), respectively. The behaviors of measured on-resistance and breakdown voltage are similar to those predicted by the simulated results shown in Fig. 5(a) and (b).

The on- and off-state *I-V* characteristics of the TLPM/S device are shown in Fig. 10(a) and (b), respectively. The TLPM/S device has a device pitch of $3.0 \,\mu\text{m}$, a channel width of $40 \,\mu\text{m}$, and an n⁻ drain dose of 7×10^{12} /cm². This device yields a drain-to-source current of 1.9 mA with $V_{\rm gs} = 20$ V and $V_{\rm ds} = 1$ V, which results in a specific on-resistance of $62.0 \,\mathrm{m\Omega} \cdot \mathrm{mm}^2$.

Fig.9 Measured specific on-resistance and breakdown voltage for TLPM/S



Fig.10 Measured I-V characteristics of TLPM/S



The device has a breakdown voltage of 72 V. The specific on-resistance is also reduced to $53.0 \text{ m}\Omega \cdot \text{mm}^2$ without sacrificing the breakdown voltage by optimizing the conditions of the p⁻ body and n⁻ drain ion implantations.

6. Conclusion

A new Trench Lateral Power MOSFET device with a trench bottom source contact (TLPM/S) was proposed, fabricated, and characterized. As is shown in Fig. 11, the TLPM/S device has improved the trade-off between breakdown voltage and specific on-resistance as compared with planar-type LDMOS devices. The TLPM/S device has also achieved higher switching performance than either that of the TLPM/D or planartype LDMOS.

Future work includes development of a new process for integrating the TLPM/S with CMOS devices to realize higher performance power ICs. This will provide portable electronic appliances with a smaller number of components, higher reliability, and lower power consumption.

References

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Fig.11 Trade-off between specific on-resistance and breakdown voltage



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