FUJI PROGRAMMABLE CONTROLLER "FUJILOG-μTmini"

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I. INTRODUCTION

FUJILOG-μTmini is a programmable controller (hereinafter called PC) most suited to control a small scale system. This small general purpose PC developed as a lower grade model of FUJILOG-μT realizes the small dimensions, light weight, handling ease, block composition and low price.

This PC has totally employed the functions, performance, instruction words and programming method of the higher grade FUJILOG-μT. The detachable special small size program loader and conventional tool group can be connected without any modification, an input signal power supply is built in, and this PC has various other features. This PC is outlined in the following pargraphs.

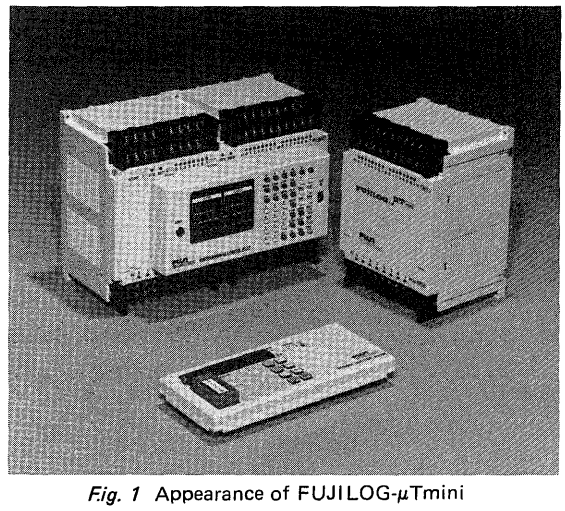

Fig. 1 Appearance of FUJILOG-μTmini

II. COMPOSITION

This PC uses a building block composition so that the most suitable system can be selected in response to each control scale. *Figs. 1* and 2 show the appearance and system configration respectively.

For the basic units, there are Model T40 which accommodates 40 input/output points and Model T40P which is equipped with an interface adapter, a conventional program tool in addition to the 40 input/output points. Up to three 24 or 16 input/output point expansion unit can be connected through the special cables, and a system of 40 to maximum 112 input/output points can be composed.

Programming is made by the special program loader (hereinafter called loader) A12T which can be attached to the basic unit directly or various program tools fur FUJILOG-μT. The loader can be operated in exactly same manner as the higher grade model FUJILOG-μT, and program processing and various monitorings during running can be made.

To keep programs, data can be recorded simply by connecting an audio cassette recorder to the special loader. It is also possible to write contents of the program memory in the basic unit into the PROM by connecting the special PROM writing adapter (A03M) instead of a loader. These special tools can be operated by using an extension adapter (A00M) and by drawing it with a cable.

Into the basic unit, the CPU, program memory and power supply unit are accommodated, and by attaching each one sheet of input/power supply card and input card with terminal block and two sheets of output card further, a system of 40 input/output points is composed. On the front face, loader and other attachment connecting portion exists, When these attachments are connected mechanically, the electrical connection completely simultaneously, and the system can be operated immediately. For Model T40P, the conventional programming tool connecting connectors are arranged in the left side.

Next, by attaching PROM to the socket located inside the cover in the front left protion, ROM operation is attained. For the PROM writing, not only the special adapter (A03M) but also the conventional tools can be applied as they are.

The input/output unit can be handled as an independent card, and selection can be made freely in response to the required specifications. Further, replacement can be made in the unit of a card, improving the maintenanceability.

III. SPECIFICATIONS AND FUNCTIONS

1. Specifications

Table 1 shows the specifications of this PC.

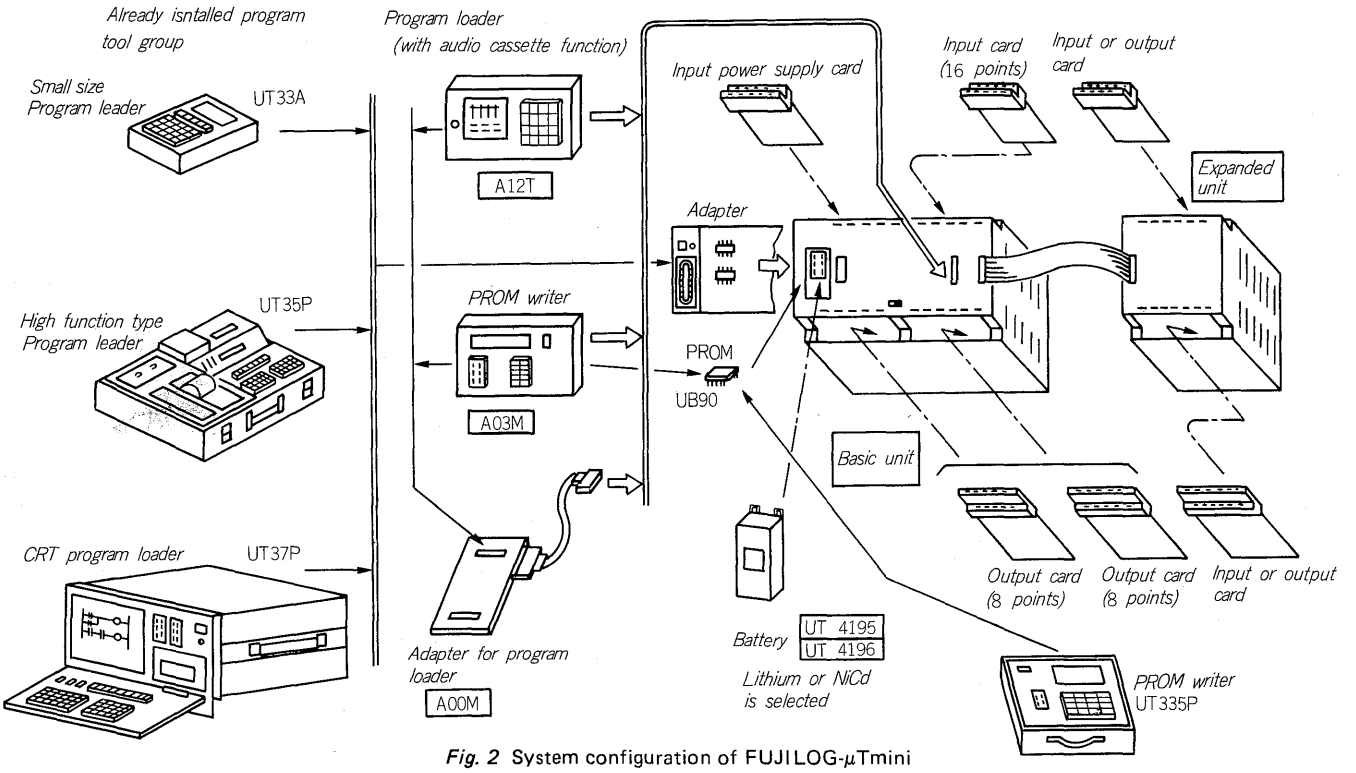

Fig. 2 System configuration of FUJILOG-μTmini

Table 1 Specifications of FUJILOG-μTmini

Item		Specification		
Program system		Stored program		
Control system		Cyclic operation		
Cycle time		About 20 msec (1024 words): Approximately proportions to program		
Type of instruction		R, A, O, W, MRG, NRG, TMR, CTR, SR, SC		
Program capacity		1024 words		
Memory element		CMOS RAM (Backed up with the capacitor. Double back with NiCd or lithium battery can also be made)		
Internal data memory	Input/output relay	112 points (buffer memory)		
	Auxiliary relay	272 points: for 34 cards (8 points per card)		
	Keep relay	128 points: for 16 cards (8 points per card) . . . . . with backed up by capacitor and battery.		
Number of control I/O points		Basic unit	Input: 24 points (fixed), Output: 16 points (fixed)	Total number of maximum I/O points: 112
		Expanded unit	Maximum number of points is 24. (Input: 16 points, Output: 8 points. However, for output, maximum number of points per unit is limited to 16.)	
Cassette		• Commercially available cassette tape recorder, FSK system • T40P is a loader for FUJILOG-μT: UT33A, UT35P, CRT loader: UT37P can be used		
Self-diagnosis		Watch dog timer, parity error, battery failure, voltage drop and program check		
Control output		STX: la contact output (ON during normal operation), BAT: la contact output (ON when battery fails or voltage drop)		
Power supply		AC100/110V Commonly used (−15~+10%) 50/60Hz		
Power consumption		Maximum 100VA (Basic system: 70VA, 10VA per expanded unit)		
Ambient temperature		0~50°C		
Keeping temperature		−10~70°C		
Ambient humidity		10~85%RH (Without condensation)		
Atmospheric condition		No corrosive gas exists		
Vibration		JISC-0911 IIB Class 3		
Noise-resistance		1000V 1μs Noise simulator		
Dielectric strength		AC1500V 1 minute, Overall external terminal-Sequencer installing plate		
Insulation resistance		DC 500V 10MΩ or more Overall external terminal-Sequencer installing plate		
External dimensions (mm)		T40P: 300 T40 : 260 (W) x 182(H) x 153(D) (Basic unit + Program loader)		
		130(W) x 182(H) x 117(D) (Expanded unit)		
Weight (kg)		T40P: Basic system (type R): 2.8, Expanded system (Type R): 0.85, Program loader: 0.36		

2. Functions

Fig. 3 shows the fundamental composition of this PC. As seen in this figure, this PC consists of three blocks, namely, the basic unit, extended unit, and program loader.

Functions and operations of each block are explained below.

1) Basic unit

The CPU is an 8-bit micro-processor which, together with the clock generator circuit, interval timer circuit, system program memory and peripheral circuits, composes the heart of this system, controlling the all the units which compose this system and performing sequence arithmetic processing.

The user program data memory is store sequence programs prepared by the user and sequence processing data, and for the program data memory, CMOS IC backed up by a capacitor having a large capacity is used. The self-discharging of the capacitor is so minor that it keeps memory contents even if the power fails. Further, when it is desired to keep the memory contents toward a longer period of time, they can by kept for several years by using a lithium battery. For these capacitor and battery, the system supervises for voltage drop and disconnection of the battery, and when voltage drops below the certain level or battery is disconnected, contact signal is sent out through the internal bus and input/output interface. As described above, the use program of this PC uses RAM together with the program memory, and when EPROM is used as a program memory, EPROM chip is installed additionally.

On the other hand, as a user program arithmetic processing method, so called compiler system is used, allowing a high speed arithmetic processing.

To be more specific, whenever the PRG-RUN switch of the basic unit is set to the RUN mode, the internal CPU converts all the user program contents to instruction words which can be processed under a high speed, and developes them to the system memory.

As for the actual sequential arithmetic processing, a high speed arithmetic processing is accomplished by executing the converted contents.

2) Input/output card and interface unit

Through the input/output card and interface unit, the basic unit is connected to external input/output signals, and they function to covert high power level signals and internal logic level signals.

The input card is provided with a photocoupler to insulate it from the outside so that the noise resistance can be improved during the level conversions. External inputs are supplied from the terminals of the input power supply card. When the built-in DC 24V power supply is used, input can be supplied simply by connecting the contacts. Further, those equipment having open collector transistor outputs can be also be connected.

For the output card, three types of output, namely, AC contactless relay (SSR) output suited to switching elements such as solenoid valve which makes and breaks

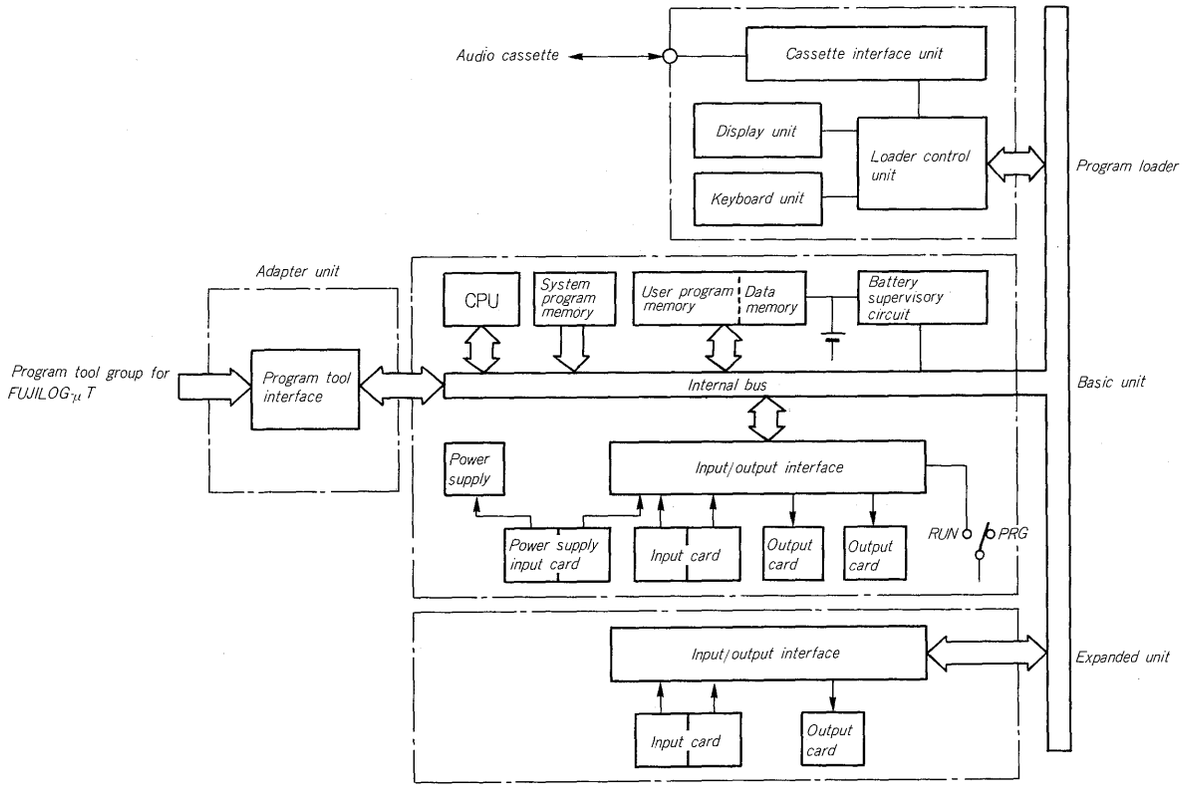

Fig. 3 Block diagram of FUJILOG-μTmini

very frequently, general purpose contact relay contact output having a cost merit, and transistor output for DC load can be selected.

The card is equipped with 8 or 16 point input and 8 point output circuits, and by the screw terminal on the front face, the card is connected to the outside.

The interface circuit functions to decide input/output card address and to latch output signals. Further, the interface circuit is provided with indicator lamps so that status of input/output signals can be checked at the front face.

Table 2 shows specifications of the input/output card.

3) Special program loader

The program loader consists of an audio cassette recorder interface for recording user programs, control switches, display LEDs and keyboard required for processings such as programming and monitoring. These components are controlled by the CPU of the basic unit through the internal bus.

The layout of keys on the front face of the loader, names, operating sequence, display, etc. are unified with those of the loader of FUJILOG-μT. The loader can be detached or attached even during running, and program can be changed or monitored. Further, for those audio cassette recorders available in the commercial markets, recording and playing can be made under FSK (Frequency Shift Keying) system, and user programs can be kept in cassette tapes. These tapes are interchangeable with other programming tool (UT 335P).

On this loader, various self-diagnosing results are displayed under each operation mode of the PC. For example, when loader operating error, parity error, etc. occur, they are displayed by each factor. *Table 3* shows the displayed contents.

4) Interface unit of the conventional program loader.

The interface of the program tool for FUJILOG-μT is installed on the Model T40P basic unit. This interface unit is accessible to the user program data memory in the manner of DMA for the internal bus, and the interface unit can be operated without affecting execution of the basic unit.

IV. PROGRAMMING

Since the instruction words of this PC are same as those of the higher grade FUJILOG-μT, refer to page 15 through 20 for FUJILOG-μT under a separate cover, for the types of instruction word and programming method. However, the scale is reduced in this PC, and program, address of each input/output relay and capacitty differ, and these factors must be taken into considerations when transferring the program. *Table 4* shows address segment and *Fig. 4* shows data memory map of this PC. All of these are handled under decimal system. The input/output addresses of the basic unit are fixed, and with the input/output compositions of the next expanded unit, input/

Table 4 Memory address of FUJILOG-μTmini

Name		Address	Remarks
Program memory		0~1023	1024 words
Data memory	Input	0.0~2.7	24 points (fixed) Basic
	Output	3.0~4.7	16 points (fixed) unit
	Input/output	5.0~13.7	Maximum 72 points Expanded unit
	Data memory	14.0~63.7 (48.0~63.7)	(Non-volatile domain)

Table 2 Specifications for I/O card for FUJILOG-μTmini

Type	System		Voltage/Current
Input power supply	Input: Non-voltage contact input Output: Relay contact output	8 points 2 points	DC 24V/10mA AC 220V/2A
Input	Non-voltage contact input	16 points	DC 24V/10mA
Relay output	Non-voltage relay contact la	8 points	AC 220V/2A
SSR output	Triac	8 points	AC 80~220V/2A
Transistor output	Open collector transistor	8 points	DC 19~60V/2A

Table 3 Various alarm indicators of FUJILOG-μTmini

Alarm indication number	Error	Explanation
Err0	Instruction word error	Undefined instruction word writing
Err1	Control error	Wiring during running, mode switch (RUN/PRG) operation during audio cassette recorder processing
Err2	Program memory error	Error of internal program memory chip, etc.
Err3	Instruction word parity error	Changed bit of instruction machine word
Err4	Instruction word format error	Abnormal change of format of instruction machine word
Err5	I/O transfer error	Abnormal data transfer with I/O unit
Err6	Expanded unit composition error	Disconnected cable of expanded unit, or additional connection during operation
Err7	Battery fault	Dropped battery voltage or disconnected cable.

Card address	Bit address								
0	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	Basic unit input unit
1	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7	
2	2.0	2.1	2.2	2.3	2.4	2.5	2.6	2.7	
3	3.0	3.1	3.2	3.3	3.4	3.5	3.6	3.7	Basic unit output unit
4	4.0	4.1	4.2	4.3	4.4	4.5	4.6	4.7	
5	5.0	5.1	5.2	5.3	5.4	5.5	5.6	5.7	Expanded unit input/output unit
6	6.0	6.1	6.2	6.3	6.4	6.5	6.6	6.7	Maximum 24 points per unit (Input: 16 points, Output: 8 points). In case of output only, however, 16 points apply, and input/output addresses are automatically decided by moving them to one side.
7	7.0	7.1	7.2	7.3	7.4	7.5	7.6	7.7	
8	8.0	8.1	8.2	8.3	8.4	8.5	8.6	8.7	
9	9.0	9.1	9.2	9.3	9.4	9.5	9.6	9.7	
10	10.0	10.1	10.2	10.3	10.4	10.5	10.6	10.7	
11	11.0	11.1	11.2	11.3	11.4	11.5	11.6	11.7	
12	12.0	12.1	12.2	12.3	12.4	12.5	12.6	12.7	
13	13.0	13.1	13.2	13.3	13.4	13.5	13.6	13.7	
14	14.0	14.1	14.2	14.3	14.4	14.5	14.6	14.7	
15	15.0	15.1	15.2	15.3	15.4	15.5	15.6	15.7	
16	16.0	16.1	16.2	16.3	16.4	16.5	16.6	16.7	
17	17.0	17.1	17.2	17.3	17.4	17.5	17.6	17.7	
									Internal data memory domain
45	45.0	45.1	45.2	45.3	45.4				
46	46.0	46.1	46.2	46.3	46.4	46.5	46.6	46.7	
47	47.0	47.1	47.2	47.3	47.4	47.5	47.6	47.7	
48	48.0	48.1	48.2	48.3	48.4	48.5	48.6	48.7	
49	49.0	49.1	49.2	49.3	49.4	49.5	49.6	49.7	
50	40.0	40.1	40.2	50.3	50.4	50.5	50.6	50.7	
51	41.0	41.1	41.2	51.3	51.4	51.5	51.6	51.7	
52	42.0	42.1	42.2	52.3	52.4	52.5	52.6	52.7	
53	43.0	43.1	43.2	53.3	53.4	53.5	53.6	53.7	
54	44.0	44.1	44.2	54.3	54.4	54.5	54.6	54.7	
55	45.0	45.1	45.2	55.3	55.4	55.5	55.6	55.7	Internal memory non-volatile domain.
56	46.0	46.1	46.2	56.3	56.4	56.5	56.6	56.7	
60	60.0	60.1	60.2	60.3	60.4	60.5	60.6	60.7	
61	61.0	61.1	61.2	61.3	61.4	61.5	61.6	61.7	
62	62.0	62.1	62.2	62.3	62.4	62.5	62.6	62.7	
63	63.0	63.1	63.2	63.3	63.4	63.5	63.6	63.7	

Fig. 4 Data memory map of FUJILOG-μTmini

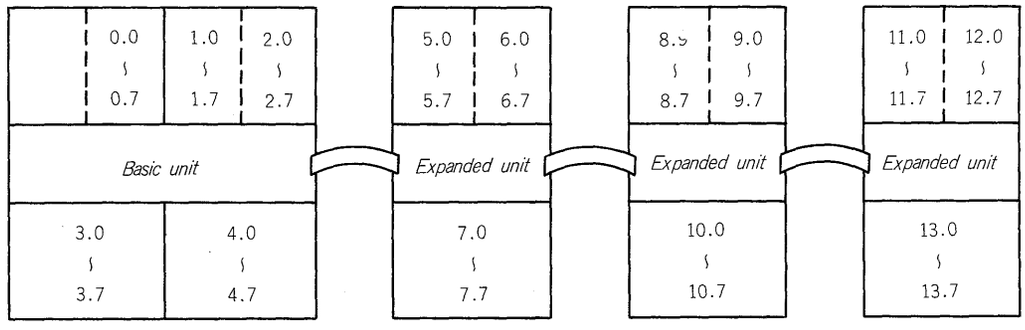

Fig. 5 I/O unit number allocation of FUJILOG-μTmini

output addresses are automatically and sequentially decided. *Fig. 5* shows input/output addresses which apply when three expanded units of 16 input points (upper portion) and 8 output points (lower portion) are connected.

V. POST SCRIPT

Presently, PC application range has been extended into small scale systems, and in response to the trend, this PC has been manufactured to expand the applications into the small scale systems with its performance and low cost.

The case is of a molded type, the construction is of a block type, and using rigid terminal block in the input/output unit, this PC has an image of the conventional electric equipment. Without having people felt electronic equipment, this PC can be handled easily by anyone.

In compariosn with the higher grade model FUJILOG-μT, the specifications and functions are sufficiently equivalent. These have been realized by development of the system of the system program which sufficiently draws out functions of a microcomputer, and at the same, low price PC has also been realized. As the result, PC can now be used for small scale relay control panel which was conventionally nounable to realize low price systems, and a wider application is expected.