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CONSTRUCTION AND FUNCTION OF FUJI SILICON CONTROLLED RECTIFIER CELLS

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I. PREFACE

A silicon controlled rectifier (SCR), a three terminal *PNPN* switch, has an anode, cathode and gate terminal. Its voltage-versus-current characteristics may be seen in *Fig. 1*. This device is quite similar to an ordinary gas thyratron and turns on regeneratively when tripped by a small gate trigger signal. After turn-on, an impedance of the device will be very low and the current will be essentially limited only by a load. The gate loses control after turn-on and the device can be cut off only by reducing the anode voltage to zero.

The SCR, because of its inherent small size, no filament heater requirements, low anode voltage drop, and fast switching action (compared with the ordinary gas thyratron), has many applications in the electronics industry.

However, the SCR has lower blocking abilities than the gas thyratron. Taking this into account, we worked on the extension of blocking abilities and now the forward and reverse blocking voltage of our device reach over 1000 v, and reverse surge breakdown voltage of 2000 v.

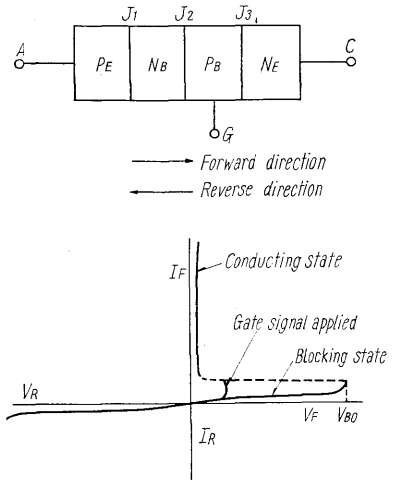

Fig. 1 Schematic and V–I characteristic of an SCR

The purpose of this paper is to explain the construction, fabrication, function and electrical characteristics of developmental devices of Fuji SCR.

II. PRINCIPLE OF OPERATION

1. Forward Direction

1) Blocking state

If the voltage is placed in forward direction across the anode and cathode terminal under open gate condition, junctions J_1 and J_3 become slightly forward-biased and a center junction J_2 becomes reverse-biased. Under these conditions, the current which flows through the device is [1]

$$I=\frac{I_{CO}}{1-M_P\alpha_{1N}-M_N\alpha_{2N}} \quad \cdots\cdots\cdots\cdots (1)$$

where α_{1N} is the fraction of the current at J_1, which is collected at J_2 as minority carrier current, and α_{2N} is the fraction of the current at J_3 which is collected at J_2. The avalanche multiplication factors for holes and electrons are given by M_P and M_N respectively. I_{CO} is the current that would flow through J_2 if it were reverse-biased, and isolated.

If $M_P\alpha_{1N}+M_N\alpha_{2N}$ is smaller than unity, the current that flows is essentially of the order of magnitude of I_{CO}. This condition is satisfied when the voltage of the center junction is appreciably less than its breakdown voltage, called the blocking state.

2) Breakover

If the voltage across the anode and cathode is increased, $M_P\alpha_{1N}+M_N\alpha_{2N}$ becomes equal to or greater than unity depending on the following two factors:

(1) The increase of electric field in the base regions N_B and P_B results in a increase of M_P and M_N.

(2) The electric field extends from J_2 into the base regions, and this results in a decrease of the effective base widths and a subsequent increase of α_{1N} and α_{2N}.

Then equation (1) is invalid and the current that flows is limited essentially by the external circuit. The voltage where $M_P\alpha_{1N}+M_N\alpha_{2N}=1$ is satisfied is called the breakover voltage.

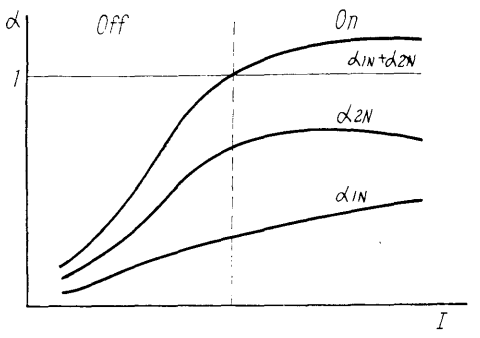

Fig. 2 α as a function of current in an SCR

The physical model of the breakover may be described as follows: as the outer two junctions J_1 and J_3 are forward biased, minority carriers are injected from each junction. If these carriers do not decrease sufficiently by recombination during a transit across the base regions N_B and P_B, these carriers may accumulate in the neighborhood of J_2. Thus the blocking ability of J_2 vanishes and turns into a conduction state.

The SCR can also be switched on by passing into the gate terminal a positive current larger than a certain specified value, even when the anode to cathode voltage is much less compared to the breakover voltage. *Fig. 2* shows current multiplication factors α_{1N} and α_{2N} as a function of current that flows through J_1 and J_3 respectively. Now, if the current that flows in the device is a magnitude of the order of I_{CO}, α's have values of the off region. Increasing the current by the gate signal increases α's according to *Fig. 2*, and even under the condition of $M_P=M_N=1$, the relation

$$M_P\alpha_{1N}+M_N\alpha_{2N}\geqq 1$$

is satisfied easily, leading to the conduction state.

3) Conduction state

In the case of conduction state, many carriers are injected into the base regions so that it resembles a rectifier under conduction state. The forward voltage drop across the device is

$$V\simeq\frac{1}{\beta}ln\frac{I_{S2}}{I_{S1}\cdot I_{S3}}\cdot I\cdot\frac{1}{\alpha_{1N}+\alpha_{2N}-1}+R_oI \quad .....(2)$$

where $\beta=q/kT$. I_{S1}, I_{S2} and I_{S3} are the saturation current of J_1, J_2 and J_3 respectively, with the other two junctions shorted. R_o is the ohmic series resistance of the end regions.

Let (2) be compared with the following, the forward voltage drop of the rectifier,

$$V\simeq\frac{1}{\beta}ln\frac{I}{I_S}+R_oI \quad .....(3)$$

one finds that (2) is essentially the same to (3) except when

$$\alpha_{1N}+\alpha_{2N}-1\simeq 0 \quad .....(4)$$

(4) is satisfied and the forward voltage drop of the SCR becomes larger than that of the rectifier only when the forward current is very small.

2. Reverse Direction

If the voltage is placed in reverse direction across the device, junctions J_1 and J_3 become reverse-biased and the center junction J_2 becomes slightly forward-biased. This differs in the case of forward-bias at the point where the forward-biased emitting junction exists on only one side of the reverse-biased collecting junctions. Since $\alpha<1$ for each base region is as shown in *Fig. 2*, carriers cannot accummulate at these points. Thus J_1 and J_3 do not lose blocking ability. The practical device, however, consists of a relatively narrow P_B region and a wide N_B region with its relatively high resistivity so as to block almost all of the reverse voltage at J_1.

We will next consider the blocking ability of J_1 as compared with a common rectifier.

When a rectifier with a $PI\!IN$ structure is reverse-biased, a space charge layer on the $I\!IN$ junction extends into the $I\!I$ region with increasing voltage, and finally breaks through to the $PI\!I$ junction. A field distribution for this case is shown in *Fig. 3 (a)*. As both ends of the space charge layer terminate in the regions of different conduction type, the blocking ability holds, and it blocks the reverse bias until a field strength at the $NI\!I$ junction reaches a critical value E_B.

However, if the space charge layer on J_1 of the SCR extends into the base region and finally breaks through to J_2, both ends of the space charge layer terminate in the same conduction type regions, and a steep increase in the leakage current appears[2]. The limiting voltage is called a " punch through voltage ".

The field distributions in the base region for a $P_EN_BP_B$ structure are shown in *Fig. 3*, in which the space charge layer punches through just when the field strength at J_1 reaches E_B (*Fig. 3 (b)*), the space

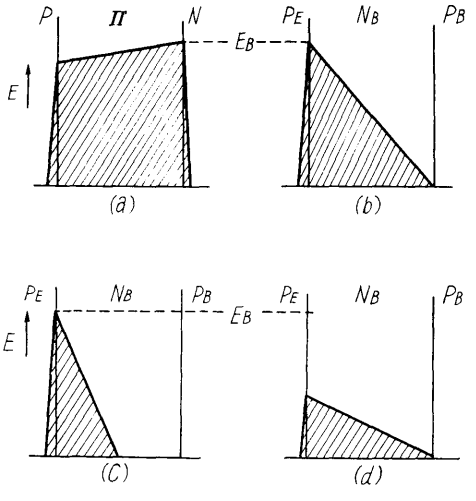

Fig. 3 Extension of an electric field in the base layer under reverse bias

charge layer does not punch through even when the field strength at J_1 reaches E_B (*Fig. 3 (c)*), and the space charge layer punches through before the field strength at J_1 reaches E_B (*Fig. 3 (d)*). It is obvious that the blocking ability of J_1 is maximum as the condition *Fig. 3 (b)* is satisfied, and the blocking voltage of the *PIIN* structure is nearly twice as large as that of the $P_EN_BP_B$ structure if both II and N_B regions have the same width.

The breakdown voltage and the punch through voltage of the $P_EN_BP_B$ transistor are shown in *Fig. 4* as a function of resistivity of N_B.[3] If the resistivity of N_B matches the cross point in *Fig. 4*, a condition of maximum voltage blocking can be satisfied.

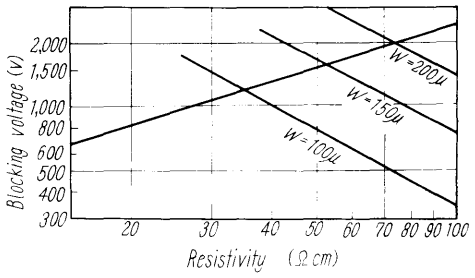

Fig. 4 Limit of a blocking ability of transistors

III. MANUFACTURE AND CONSTRUCTION

The SCR may be fabricated usually from either of next two procedures.

All diffusion type: Slices of N type silicon are subjected to solid state diffusion, the diffused layers serving both as the P type gate and the P type anode. The N type cathode is then formed by a second solid state diffusion so as to make a *PNPN* structure. Both sides of this silicon slice is then plated and the P type anode is soldered to a copper case. The cathode and gate leads are also attached and the whole is put into capsule form.

Alloy diffusion type: The *PNP* silicon slice is formed in the same way as mentioned above. The N type cathode is then formed by alloying a gold foil to one side of the diffused silicon wafer, with a gate contact near its periphery. Aluminum is used to affix the anode to a base electrode, and the latter is soldered to a copper case. The cathode and gate leads are then attached and the whole is put into capsule form.

These two types will be compared with respect to their electrical and mechanical performances as follows:

1) There is no essential difference in blocking ability of either type, since each device blocks the forward and reverse bias by the similar diffused junction J_2 and J_1 respectively. However, the forward blocking voltage relates not only a unique property of J_2, but also current multiplication factors of P_B and N_B. This is a function of the width of each region and since P_B is thinner than N_B, the width of P_B must be set up as uniform as possible. This is easily achieved in our factory by using an alloying technique which is obtained through a development of silicon power rectifiers.
2) When the device is used for a long period, a thermal fatigue between silicon slice and copper case takes place, becoming a serious problem. The alloy diffusion type has an advantage over this, since it is formed by alloying the silicon slice together with the base electrode, while the all diffusion type has relatively weak plated and soldered layers between slice and base electrode.

For these reasons, we have chosen the alloy diffusion type for our device.

Fig. 5 shows the fabrication process. As a starting

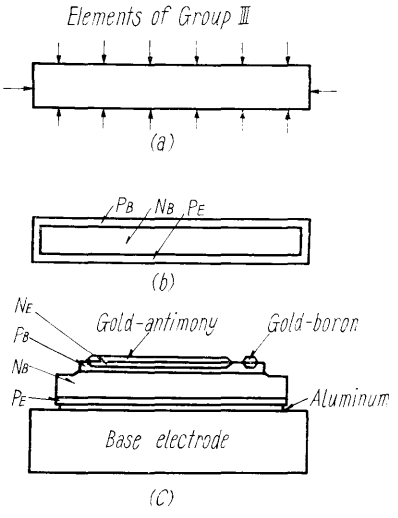

Fig. 5 Fabrication process of SCR cells

material, a 60 ohm-cm N type silicon slice is used. After boron is diffused into it, the silicon slice is cut into desired pieces and at the same time a periphery of its P_B region is removed. This silicon slice is then alloyed together with gold-antimony, gold-boron and an aluminum foil as shown in *Fig. 5*.

Fig. 6 illustrates a cross section of the device. Regions from cathode to anode (*Fig. 6 (a)*) and from cathode-gate to anode (*Fig. 6 (b)*) are shown where each junction is formed with a good uniformity. To obtain good forward and gate characteristics, it is of particular importance to make the width of P_B under the cathode uniform within a tolerance of ± few microns. The periphery of the device is removed (*Fig. 6 (c)*) as previously described. A surface leakage path from J_1 to J_2 is thus elongated, and stabilities of the device for an overvoltage

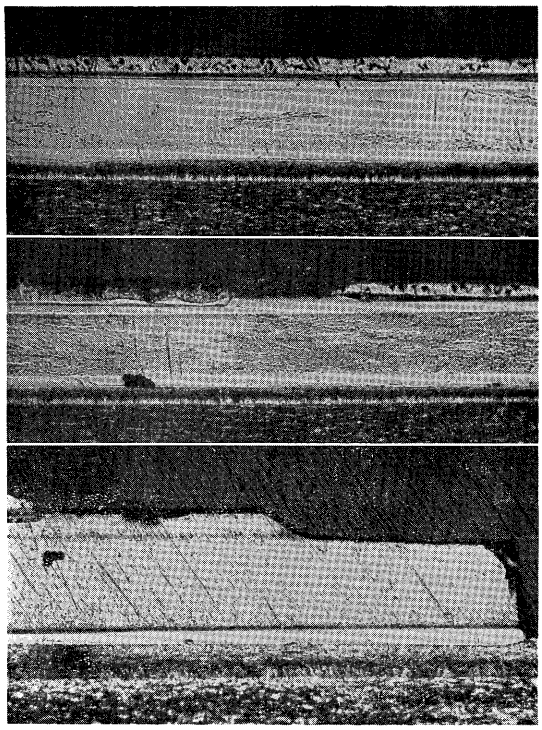

Fig. 6 Cross section of SCR

and a deterioration of blocking characteristics during severe aging tests are improved.

The element formed above is then etched and surface treated and finally put in the case. *Fig. 7* illustrates a construction of GSi 12 and GSi 150 as representatives of the SCR series in our factory. These are analogous to our silicon rectifiers Si 12 and Si 150. The base electrode of GSi 150 is larger than GSi 12, and is prone to a thermal fatigue of solder between the element and the case or lead. We have a unique construction to avoid such de- and mechanical terioration.

As mentioned above, we have established cells with high reliability with respect to both electrical and mechanical performances.

IV. CHARACTERISTICS OF SCR

1. Blocking Ability

As an example of the blocking ability, typical forward and reverse blocking characteristics of our developmental cells are shown in *Fig. 8*. The break-over voltage is greater than 1000 v in a temperature range of 25°C～125°C. Moreover, a half cycle reverse voltage up to 2000 v does not harm the device. A characteristic of this device is that the blocking voltage at 125°C is higher than that of room temperature for the forward direction as well as for the reverse direction.

Let us go into more datail.

1) Temperature dependence of the reverse blocking voltage

With increasing reverse voltage, an avalanche built up of current carrier results by collision ionization, and the leakage current increases abruptly. At lower temperature, thermal vibration of silicon lattice is small in comparison to the case of higher temperature. This leads to a small interaction between carriers and

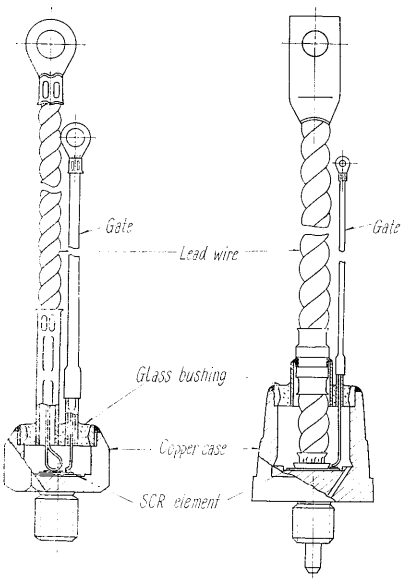

Fig. 7 Construction of GSi 12 and GSi 150

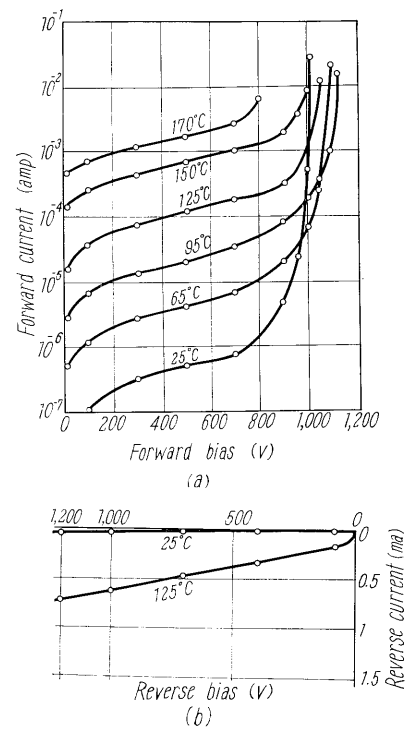

Fig. 8 Forward and reverse blocking characteristics of GSi 12

lattice vibrations which in turn increases a mean free path of carriers.

Consequently, a momentum energy of carriers at lower temperature is larger than the case of higher temperature just before collision, and a collision ionization rate at lower temperature is larger than that of higher temperature. Thus temperature coefficient of reverse breakdown voltage has a positive value. Let the reverse breakdown voltage at T_0 be $V_B(T_0)$, it is given at T as follows[2]:

$$V_B(T)=V_B(T_0)[1+8.9\times10^{-4}(T-T_0)] \quad .....(5)$$

2) Temperature dependence of the breakover voltage

At the forward direction, we must consider temperature dependence of α_{1N} and α_{2N} in addition to that of collision ionization. α_{1N} and α_{2N} increase with temperature, since an increase of the leakage current with temperature lead to an increase of α according to *Fig. 2,* and an increase of carrier lifetime with temperature results in an increase of α with temperature. To avoid a decrease of V_{BO} at higher temperature, the leakage current should be kept as low as possible, and at the same time α at a small injection level should be kept so small as to $M_P\gamma_{1N}+M_N{}_{2N}$ be smaller than unity even whenoperating temperature is high.

2. Forward Characteristic

Typical forward characteristics for the conduction state are shown in *Fig. 9.* At currents below approximately 1A/cm², the forward voltage drop actually increases slightly as the current decreases. This is due to the condition (4) as previously described.

3. Firing Characteristic

1) Steady state behavior

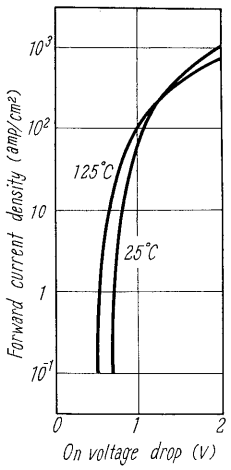

Fig. 9 Typical forward characteristic curves

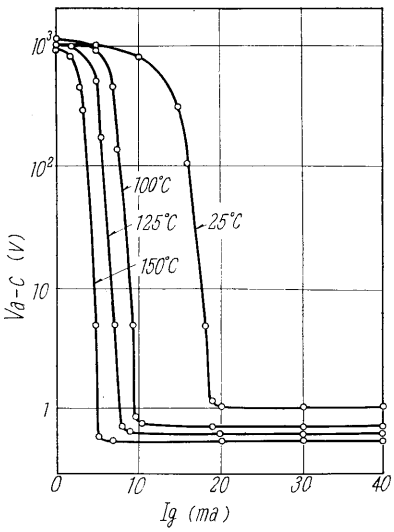

Fig. 10 Relation between anode to cathode voltage and gate current to fire

Since $M_P\alpha_{1N}+M_N\gamma_{2N}$ increases with a forward voltage V_{AC}, the minimum gate current to fire I_{GF} decreases with increasing V_{AC}. When V_{AC} is reduced below approximately 1 v, the device does not fire at any gate current. *Fig. 10* illustrates a relation between V_{AC} and I_{GF}. For small V_{AC}, the center junction may become forward-biased and γ decreases rapidly. This is similar to a case of collector current saturation in the transistor. I_{GF} of our GSi series is specified at $V_{AC}=5$ v.

2) Transient behavior

Switching speed can be specified generally using turn on time. It is a period of time required for V_{AC} to reach 10 percent of its initial value after rectangular gate signal is applied, and is given as follows.[4]

$$t_{on}=t_1+t_2+t_3+t_4 \quad .....(6)$$

t_1 is a time required for electrons injected from N_E to arrive in N_B, and t_2 is a time required for holes to arrive in P_B which is injected from P_E just after above mentioned electrons arrive in N_B. After t_1+t_2, injected electrons and holes can exist at the J_2 region, and if the gate pulse is greater than I_{GF}, they begin to accumulate. t_3 is a time required for the accumulation of injected carriers, t_4 is a delay due to a transverse spreading of turn on across the whole base region.

When a transit time of carriers is considered depending only on diffusion of them as usual, t_1+t_2 may not be less than approximately 20μ sec for our GSi series. In actual devices, however, the turn on time depends strongly on the gate current. Solid lines in *Fig. 11* illustrate them. Broken lines are also shown in the Figure. This is calculated from device parameters by author[5] through following considerations: Carriers move across the base region both by diffusion and drift where drift field in P_B arise from impurity gradient and

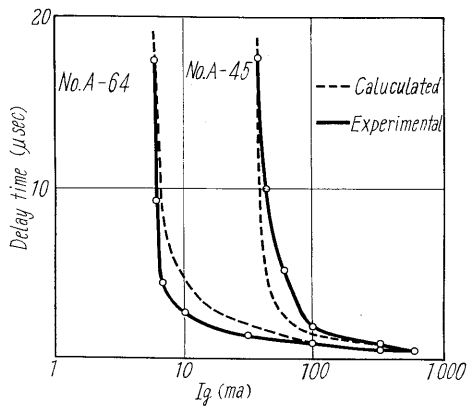

Fig. 11 Delay time as a function of gate current

that in N_B arise from majority carrier current induced by the gate signal. Thus t_1+t_2 reduces with increasing gate current. When I_G is reduced to I_{GF}, $\alpha_{1N}+\alpha_{2N}-1$ approaches zero and t_3 increases indefinitely.

In this way we can reduce a switching time by using a larger gate current than I_{GF}.

4. Turn Off Characteristic

When reverse voltage is applied to the device immediately following forward conduction, it has a low reverse impedance until the stored carriers in the end junctions are swept out. The disposal of excess carriers can be effected in two ways-one by carrier withdrawal and the other by recombination. If forward voltage is reapplied before carriers are not swept out sufficiently, the device will fire again. The device will have regained control if forward voltage is reapplied after carriers are swept out. The minimum time to regain control is called turn off time. The situation is shown in *Fig. 12*. To minimize the turn off time, it is necessary to reduce the width of the inner base regions and to reduce the lifetime throughout the device. This lowers the blocking ability. The SCR with high blocking voltage will have thus an inferior frequency response and vice versa. As mentioned above, since the turn off time is related to the mechanism of carrier recombination, it increases with temperature as shown in *Fig. 13*.

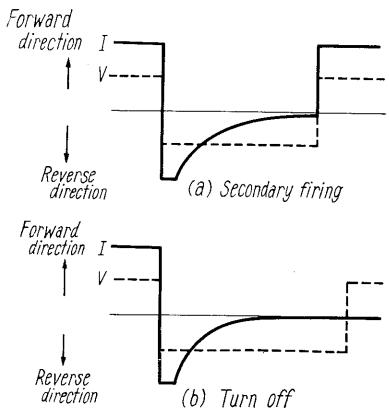

Fig. 12 Turn off characteristics

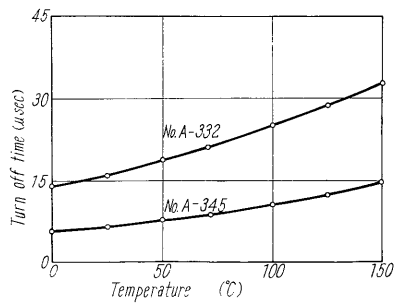

Fig. 13 Turn off time as a function of temperature

5. Reverse Leakage Current with Gate Current

If the gate trigger is applied during a reverse biased phase, an increase of reverse current with gate trigger results. This is shown in *Fig. 14*. Let

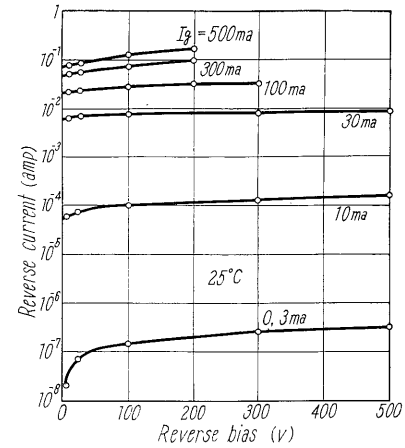

Fig. 14 Reverse current as a function of gate current

α_{1I} be a current multiplication factor of $P_BN_BP_E$ transistor with P_B emitter and injection efficiency of J_3 be equal to unity and I_{S1}, I_{S2}, I_{S3} be neglected, the increase of reverse current ΔI_R with I_G is given as follows:

$$\Delta I_R = I_G \times \frac{\alpha_{1I}\ \alpha_{2N}}{1-\alpha_{1I}+\alpha_{1I}\alpha_{2N}} \quad \cdots\cdots\cdots\cdots\ (7)$$

Typical value of $\Delta I_R/I_G$ is given in *Fig. 15*. To avoid a thermal run away by ΔI_R, I_G should be kept below about 10 percent of I_{GF} during the reverse biased phase.

6. Holding Current

When operated under conducting state, the device will return to the blocking or non-conducting state if the load current is reduced below the value designated as the holding current I_H. This is due to the reduction of α according to the curves of *Fig. 2* with reducing forward current. Since α's for these low injection levels increase with temperature (as is easily inferred from *Fig. 15*), the current which keeps

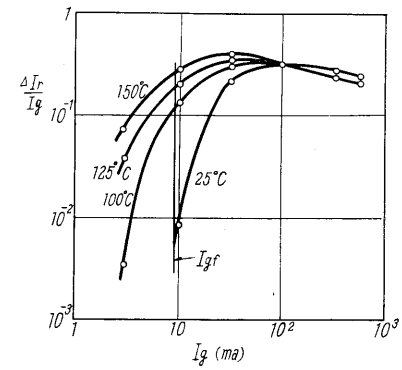

Fig. 15 Increase in reverse current as a function of gate current

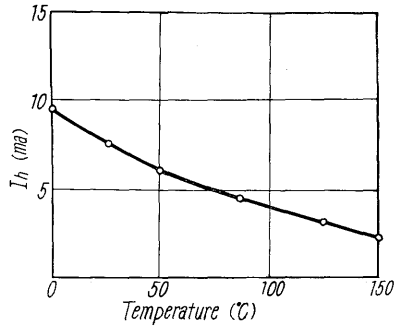

Fig. 16 Holding current as a function of temperature

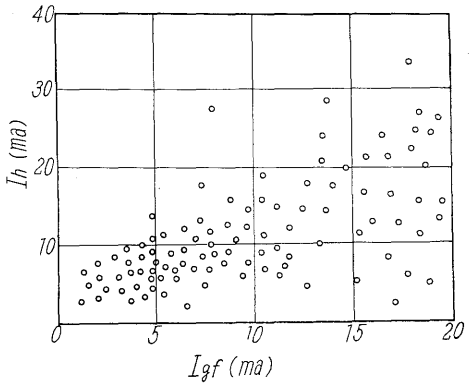

Fig. 17 Relation between holding currents and gate currents to fire of GSi 12

the same value of $\alpha_{1N}+\alpha_{2N}$ decreases with temperature. Thus I_H decreases with temperature as shown in *Fig. 16.*

I_H has also a relation with I_{GF}. Some examples are shown in *Fig. 17.* I_{GF} increases with increasing I_H since the current density to satisfy the relation $\alpha_{1N}+\alpha_{2N}\geqq 1$ is higher in the device with larger I_H.

V. SUMMARY

The construction, manufacture, and characteristics of Fuji SCR have been described: characteristics of GSi 12 are especially discussed relative to the physical and electrical characteristics of each base region.

SCR series are manufactured through an excellent manufacturing process which is developed in our factory. Their reliability is on the same level with our silicon rectifiers. SCR may be more widely used in the future than the silicon rectifier, so we are now working for still more improvements in their reliability.

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