UDC 539.23:621.382.049.774

CMOSIC TECHNOLOGY

Toshio Komori
Masato Nishizawa
Yoshiyuki Sakai

1. FOREWORD

Fuji Electric CMOSIC technology started from development of the signal transmission LSI using Al-gate CMOSIC technology of 1979 and its technical features were pursued for discrimination and applied to custom IC.

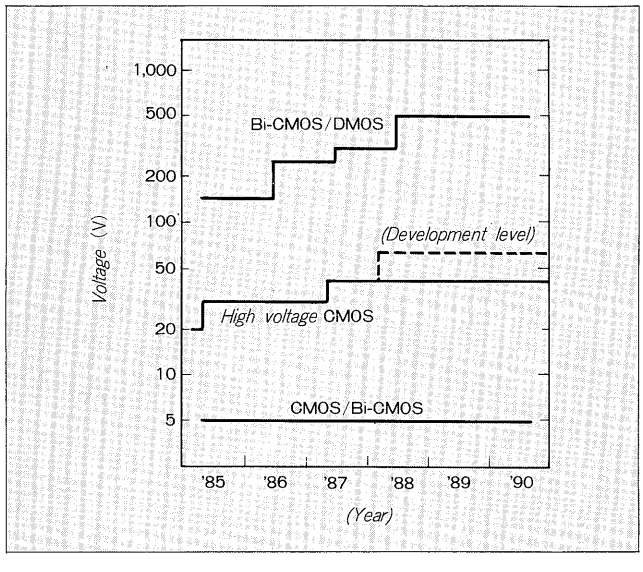
Presently, Si-gate CMOSIC technology is the main force. It features high voltage, high speed, high packing density, sensor integration, bump technology compatibility, etc. Applications to high performance custom IC cover from LCD controller-driver to custom memory and auto-focus IC.

This article introduces the high-voltage CMOSIC technology which has become the current main force technology and multi metal layer technology which allows the higher performance and high speed high packing density.

2. HIGH VOLTAGE CMOSIC TECHNOLOGY

One feature of Fuji Electric's CMOSIC technology is that combination which allows an output voltage of 10 to 40V without changing the process for the normal 5V operation substantially was realized. The progress and features of high voltage technology up to now are described below.

Fig. 1 Progress of high voltage technology



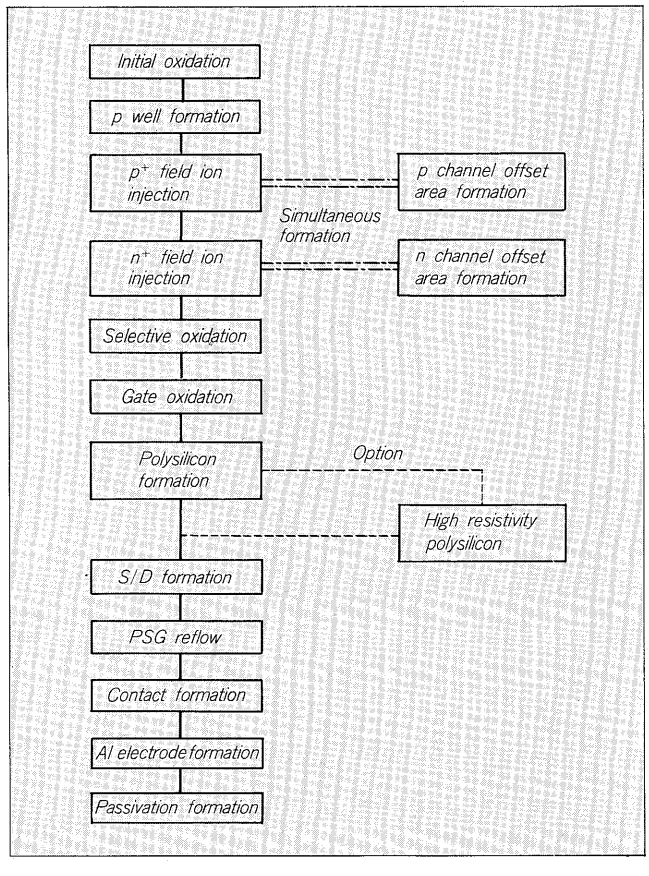
2.1 Progress of high voltage technology

The progress of Fuji Electric's IC high voltage tech-

Table 1 High voltage CMOS processes

Design rule (μm)	Power supply voltage (V)	Maximum clock frequency (MHz)	Polysilicon	Metal
6	30	8	1 layer	1 layer
4	40	15	1 layer	1 layer
2	40	20	1 layer	1 layer/ 2 layers

Fig. 2 High voltage CMOS process flow



nology by process was shown in *Fig. 1*. However, up to a maximum of 70V (development level) can be handles for a high voltage CMOS process.

When viewed from the standpoint of microphotolithography, high voltage 2μm rule CMOS process as shown in *Table 1* is achieved and operation up to a maximum of 40V is possible.

2.2 Special features of process technology

The special features of process technology will be described by taking 4μm rule high voltage CMOS technology as an example.

(1) Rationalization process considering compatibility with the ordinary CMOS process
(2) High voltage technology by offset transistor
(3) Dual conductive type polysilicon electrode
(4) High resistivity polysilicon is available by extraction implantation
(5) Gold and solder bump technology for assembling

Ion implantation for field formation for isolation and low dose ion implantation for offset formation are combined in the process flow shown in *Fig. 2*. That is, the high voltage device structure used LDD (Lightly Doped Drain) by mask alignment as shown in *Fig. 3*. Device characteristics like those described in the next paragraph are realized by skillfully balancing the voltage and drain resistivity tradeoff by optimizing the concentration and offset length of this low concentration offset area.

2.3 Device characteristics

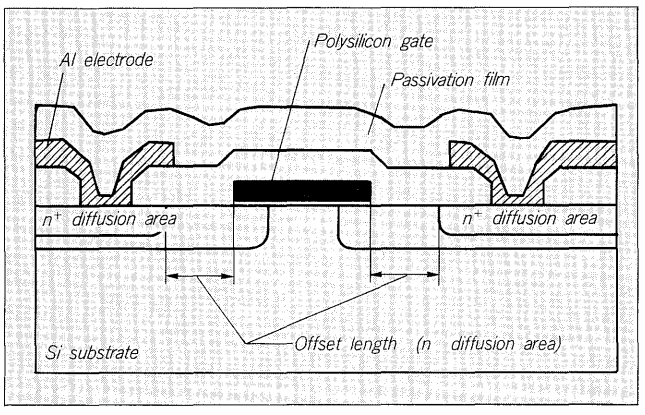
The device characteristics of the high voltage output transistor are shown in *Table 2*.

The FET voltage-current characteristic curves of an n channel and p channel transistor are shown in *Fig. 4* and *Fig. 5*.

Table 2 High voltage FET device characteristics

Item	Typical	Condition
BV_{DS}	40V	–
V_{DS}	38V	–
R_{on}	1 kΩ	V_{DS}=0.5V

Fig. 3 High voltage CMOSFET cross section



3. MULTILAYER METALLIZATION

The growth of IC microlithography and high density packing is amazing and not only shrinking of the two dimensional design rule, but also realization of high performance by making multi-layer are desired.

Fuji Electric has completed development of 2~1.5 μm rule Al double layer metallization and intends to apply it to Bip, Bi-CMOS, and CMOSIC.

The features and process of Fuji Electric Al double layer metallization are outlined.

3.1 Necessity and technical features

The necessity and technical features of Al double layer metallization are summarized below.

3.1.1 Necessity

(1) Application to ASIC and reduction of design turn around time by design automation. An example of automatic layout with the horizontal line as the 1st Al layer and the vertical line as the 2nd Al layer line is shown in *Fig. 6*. An example of the completed product is shown in *Fig. 7*.
(2) Application to high speed LSI: High packing density and high performance of Bip, Bi-CMOS, CMOS, and other ICs.

Fig. 4 High voltage channel FET voltage-current characteristics

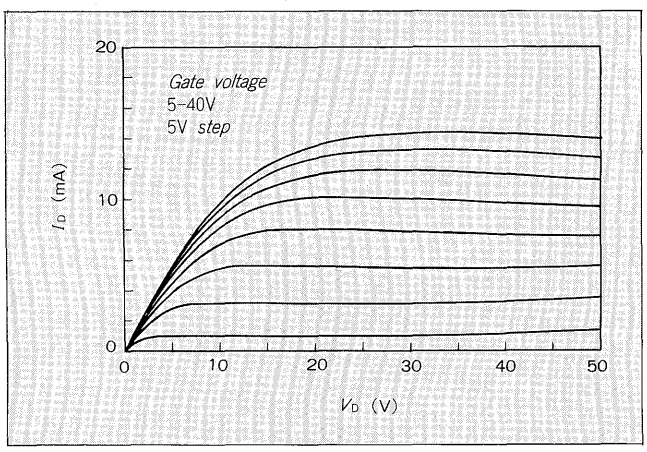


Fig. 5 High voltage p channel FET voltage-current characteristics

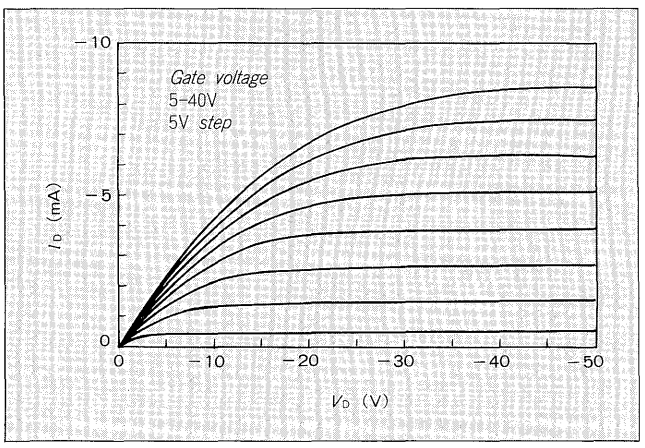


Fig. 6 Double metal interconnection layout employing automatic routing and placement

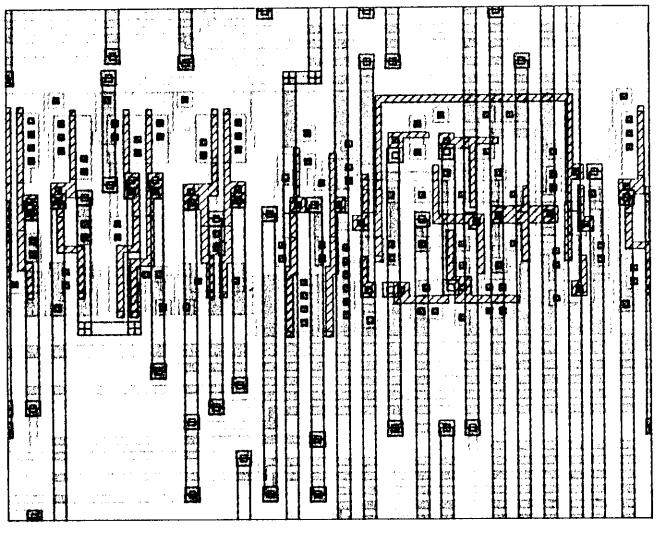
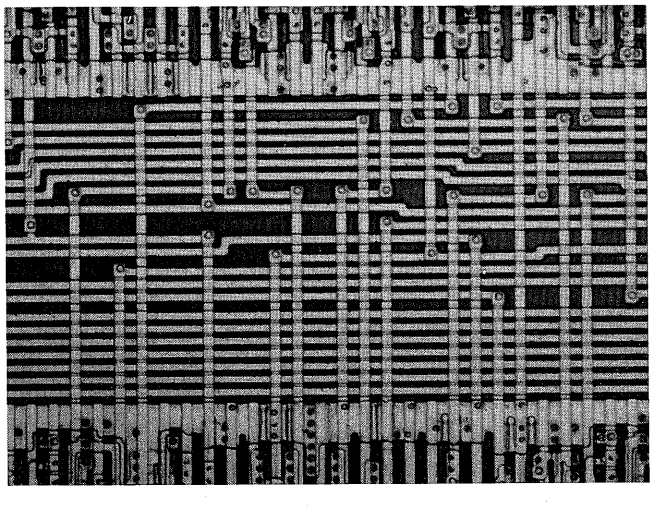


Fig. 7 Product using Al double layer interconnection



(3) Chip area reduction

3.1.2 Main technical features and problems

These are outlined in *Table 3*. For LSI multilayer metallization even though two dimensional reduction is possible, third dimension cannot be reduced greatly like plain surface scaling for the following two reasons:

(1) To improve operation speed

(2) To secure reliability

Therefore, surface roughness becomes serious and the problems shown in *Table 3* are compounded. An important technology which solves these problems is micropattern planarization.

Aiming for a high reliability process, Fuji Electric has developed the Al double layer metallizations process described below.

3.2 Planarization technology

Planarization technology for interlayer dielectric film smoothese steps produced by the bottom layer of Al and the dielectric film pattern in the chip surface. It is

Table 3 Special features of double layer metallization and problems to be solved

Technical features	Problems to be solved
Contact and anisotropic etching of metal	Microlithography
Planarized dielectric film	Improvement of reliability Escape from disconnection
High voltage, high reliability dielectric film	Escape from Al bridging by hillock
Interconnection and through hole low resistivity	High speed

Table 4 Comparison of SOG method and etch back method

Item	SOG method	Etch back method
Principle	· Spin coating of organic solution of silanol, smoothing of steps, creation of solid film by baking	· Creation of dummy insulator film on the interlayer film surface, planarizing by etching both the dummy film and convex part of the interlayer film
Advantages	· Single process · Low price	· Fewer impurities
Dis-advantages	· SOG cracking (thick film) · Organic material · Sandwich structure	· Etching accuracy depends on pattern size · Severe radiation · Poor throughput

Fig. 8 Double layer metallization process sequence cross section

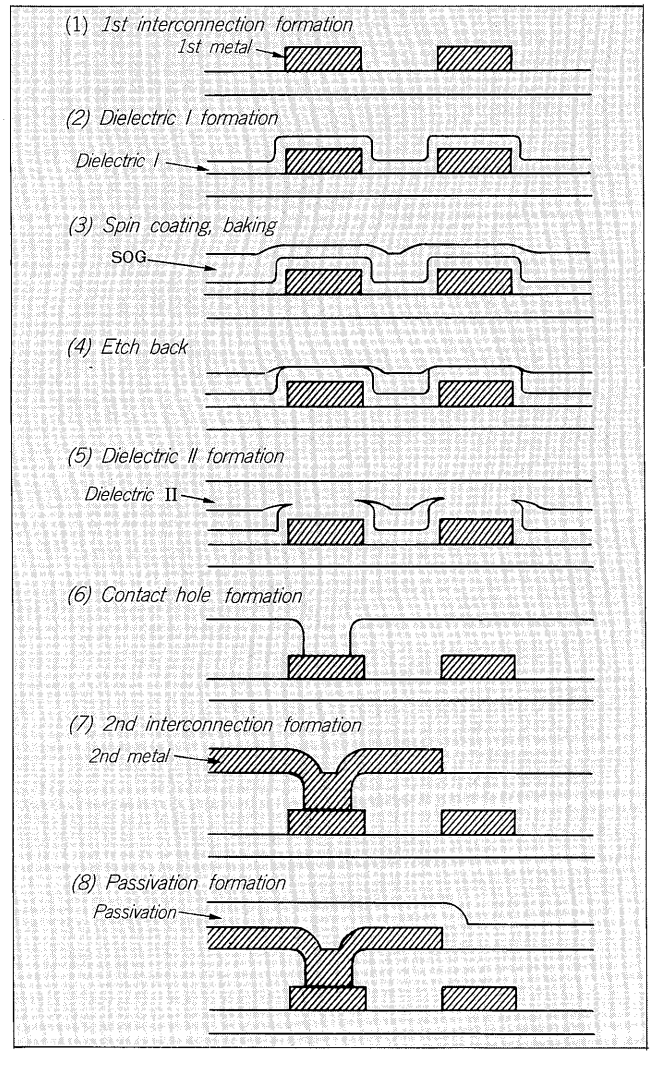


Fig. 9 Cross sectional SEM micrograph of planarizaed surface

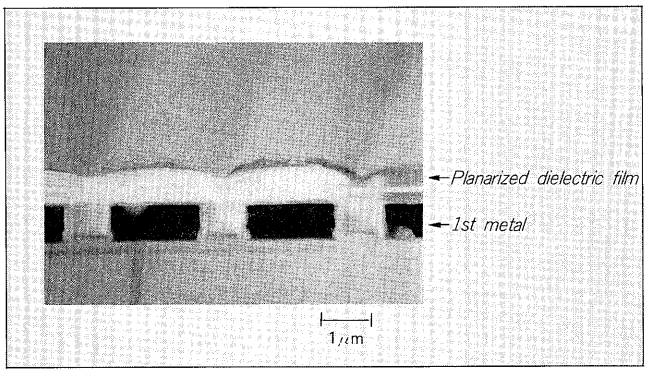
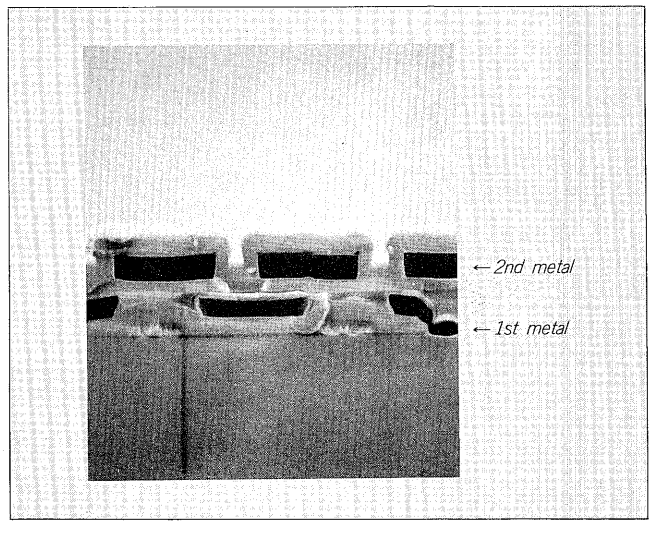


Fig. 10 Cross section micrograph of double layer metallization IC



a very important technology in the double layer metallization process.

Currently, the SOG (Spin On Glass) method and etch back method are utilized as the most practical planarization technologies. They are compared in *Table 4*.

As a result of a comparative study of the various planarization technologies, Fuji Electric adopted the SOG method with its excellent reliability and productivity. The main features of the SOG method are:

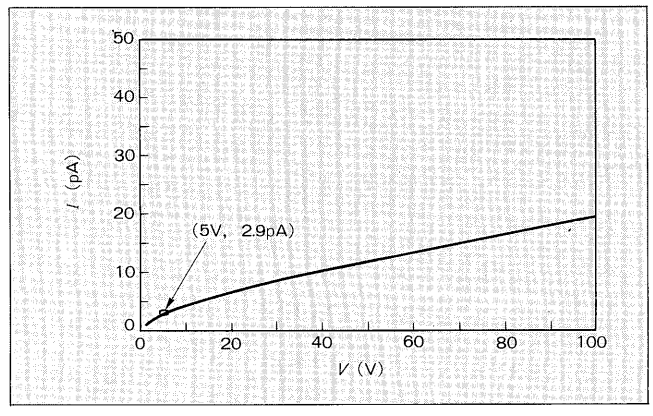
(1) Since organic SOG is used, planarizing properties are excellent.
(2) Sandwich structure including SOG as the middle layer gives high reliability.
(3) Since SOG etch back is performed, contact hole reliability is good.

3.3 Multilayer metallization process

The actual double layer metallization process is shown in *Fig. 8*.

(1) 1st connection formation
(2) Dielectric I formation
(3) SOG spin coating and baking
(4) Etch back
(5) Dielectric II formation

Fig. 11 Leakage current characteristics of interlayer dielectric film



(6) Contact hole formation
(7) 2nd interconnection formation
(8) Passivation formation

The cross sectional SEM micrograph when planarization of the steps produced by the 1st metal was performed by using the process above is shown in *Fig. 9*. It can be seen that the SOG is buried in the 1 μm space of the metal and planarization is very good.

The cross sectional SEM micrograph when this process was applied to an actual double layer metallization IC is shown in *Fig. 10*. Since the bottom step is planarized cleanly, an almost perfectly flat 2nd metal is formed.

3.4 Reliability

The following evaluation and verification were performed with process test modules to evaluate the reliability of this process:

(1) Dielectric breakdown test on interlayer dielectric film
(2) Electromigration (EM) evaluation test
(3) Contact hole resistivity evaluation test

An example of the leakage current characteristics of the dielectric film after 1000 hours withstand test is shown in *Fig. 11*. A drop of dielectric strength is not seen even after the acceleration test.

Extremely high reliability was confirmed as a result of various evaluation tests.

The Fuji Electric multilayer metallization process was described above. Up to the 1.5 μm rule double layer metallization processes is guaranteed as a total process.

4. CONCLUSION

The high voltage technology and multilayer metallization technology for Fuji Electric's CMOSIC technology were described above. As CMOSIC technology, custom processes which allow building in of a photosensor, CCD, ROM, etc. are also available.

A newly developed 6 inch wafer 1 μm CMOS process will be added to the line up. The so-called system on chip will be promoted by materializing user needs in response to the market demand for diversification and high performance and will contribute to the evolution of electronic machine systems.