Supplemental Explanation

Supplemental explanation 1 3-level inverter technology

A multilevel-type inverter, as typified by a 3-level inverter, has many advantages over a typical 2-level inverter. As shown in the Figure, the voltage waveform at the conversion output part of the 2-level inverter is $\pm E_d$ pulse width modulated (PWM) pulses centered about the zero point, but in the case of a 3-level inverter, is combined PWM pulses of $\pm E_d/2$ and $\pm E_d$ centered about the zero point. Because the output waveform of the 3-level inverter more closely resembles a sine wave, the size of the LC filter used to convert the output waveform into a sine wave can be reduced. Furthermore, the switching loss occurring in a switch element is roughly halved and the noise generated by the equipment is also reduced, because the width of voltage fluctuation per one-time switch operation is half that of the 2-level inverter. The use of a 3-level inverter having these characteristics is effective for realizing smaller size and higher efficiency in a system.

For 3-level inverters, the method shown in the Figure in which an inverter is wired to the intermediate potential (N) of the DC power source, is known as the neutral-point-clamped (NPC) method. The naming of this method originates from the fact that the voltage applied to the switch element is always clamped to half the DC voltage E_d.

Compared to the NPC method, the advanced-NPC (A-NPC) method enables a simpler circuit configuration because the series-connected insulated gate bipolar transistors IGBTs have twice the rated voltage as the IGBTs used with the NPC method, and an reverse blocking IGBT is connected between the intermediate potential point (N) of the DC power source and an intermediate point (U) of the series-connected IGBTs. Having fewer current-conducting elements, the A-NPC method has the advantages of realizing lower loss and, when configuring the inverter, of requiring fewer number of power sources for the gate driving circuit.

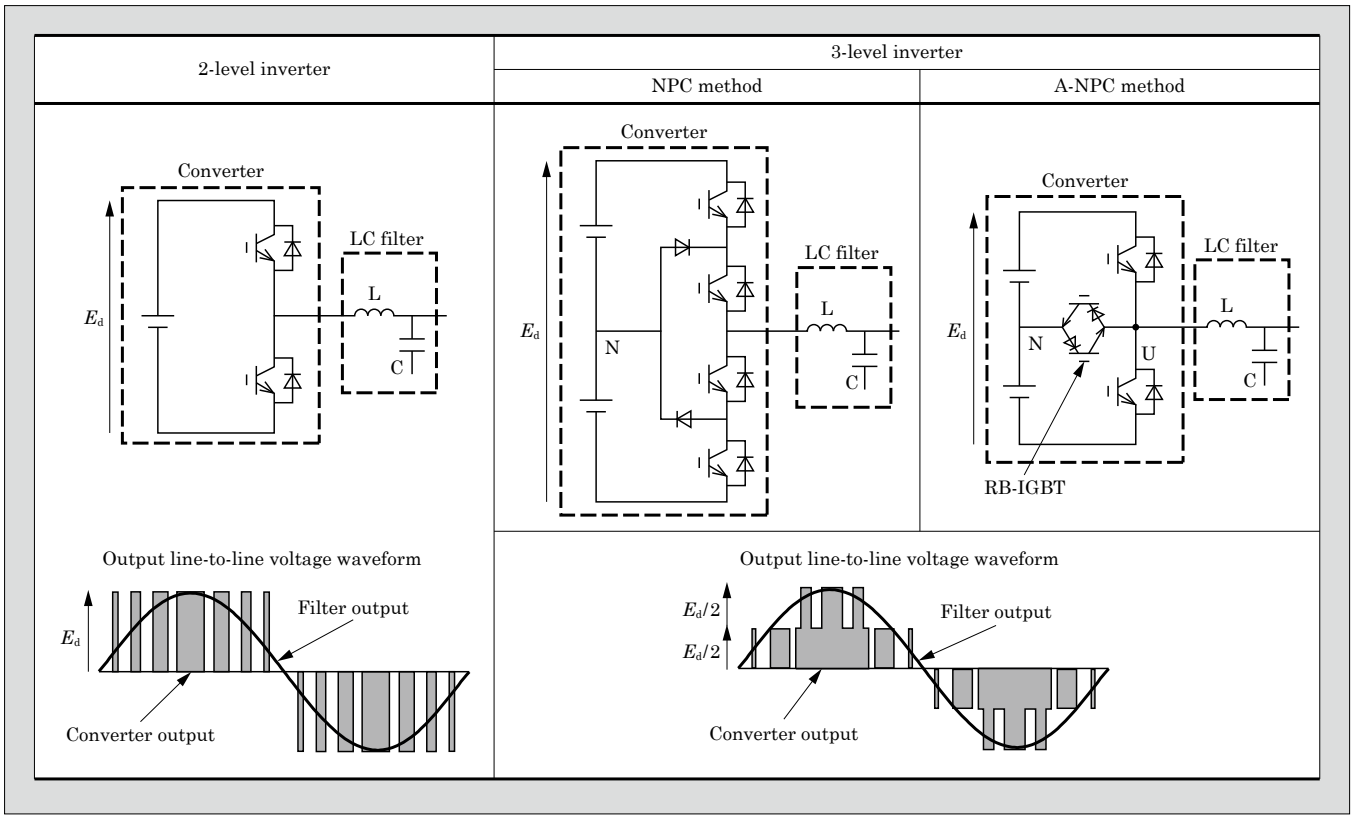

Figure Comparison of 2-level inverter and 3-level inverter circuits and voltage waveforms

Supplemental explanation 2 Miller period

In the switching of a semiconductor device, the gate capacitance is charged and discharged to turn-on and turn-off the device. At such times, changes in the drain-source voltage V_{DS} cause the gate-drain capacitance C_{GD} to change, and an interval occurs in which the gate-source voltage V_{GS} for charging and discharging C_{GD} becomes flat. This is known as the Miller period. The Figure shows a schematic of the L-load turn-off switching waveform of a power metal-oxide-semiconductor field-effect-transistor. As shown in Figure, when V_{GS} decreases, at the time t_0 when $V_{GS}=V_{DS}$, a depletion layer begins to expand on the gate to the drain and V_{DS} begins to increase. As a result, C_{GD} decreases and the Miller period is appeared. At the time t_1 when V_{DS} reaches the power source voltage, the depletion layer has stopped to expand, C_{GD} stops decreasing and the Miller period ends. At the end of the Miller period, V_{GS} and the drain current ID begin to decrease. The duration of the Miller period depends on the product C_{GD} and the gate resistance R_g, and therefore it is important that the device be designed such that loss does not increase with an extended Miller period.

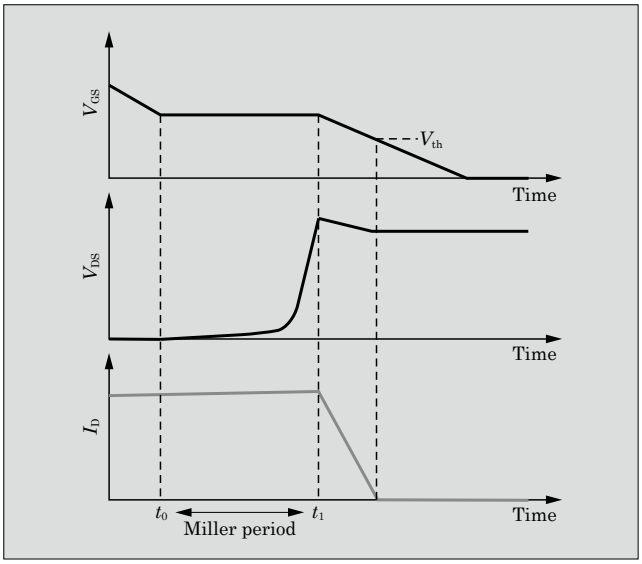

Figure Schematic diagram of L-load turn-off switching waveform