# Auto-Zero Amplifier Technology for Intelligent Power Switches

IWAMOTO, Motomitsu* TOYODA, Yoshiaki* KATAKURA, Hideaki*

**ABSTRACT**

Electronic components installed in an automobile have recently increased in number and are therefore being required to be mounted with high density on the electronic control unit (ECU) board. They are also required to be miniaturized and integrated. Fuji Electric has therefore been studying the development of a next-generation intelligent power switch that integrates current drive devices, current-sensing amplifier, and a current detection shunt resistor into a single chip. Integrating a shunt resistor into the chip requires an amplifier with enhanced accuracy. We have thus developed a highly accurate auto-zero amplifier technology that automatically corrects output errors. This amplifier helps reduce the ECU board footprint while maintaining the same current detection accuracy as conventional products.



## 1. Introduction

In recent years, there has been strong demand for improved environment, safety, and comfort in automobiles. In terms of the environment, efforts are being made to improve the fuel efficiency and electrification of vehicles. In terms of safety, initiatives are being taken to promote autonomous driving, including advanced driver assistance systems. As for comfort, measures are being adopted to reduce the size of components to ensure larger interior space.

Fuji Electric has developed intelligent power switches (IPSs)[1),2)], pressure sensors[3)], and igniters for automotive power ICs. IPSs are used as a current-drive device to drive solenoid valves for controlling transmissions. Reducing the size of IPSs and integrating peripheral components into a single chip enable miniaturization of the electronic control unit (ECU) board, which contributes to improved comfort by creating larger interior space. Improvement in the accuracy of IPS current detection also enables highly accurate control of the transmission, leading to high fuel efficiency.

Although miniaturization of the ECU board can be achieved by integrating the IPS and a shunt resistor for current detection into a single chip (instead of installing them separately), this increases the error of the current-sensing amplifier output and results in lower current detection accuracy. To solve this problem, we have developed an auto-zero amplifier technology that can prevent increase in output error even if the IPS and shunt resistor are integrated into a single chip. In this paper, we will provide an overview of the technology and describe some applications.

* Semiconductors Business Group, Fuji Electric Co., Ltd.

## 2. Challenges Related to Linear IPSs

### 2.1 Features of a linear IPS

IPSs are power ICs that add various control functions to power metal-oxide-semiconductor field-effect transistors (MOSFETs). Among the IPSs is a linear IPS that has a built-in amplifier that senses the current flowing into the load. Figure 1 shows the usage of Fuji Electric's conventional linear IPS.

A linear IPS supplies current to a load based on commands from a microcomputer. A shunt resistor converts the current into a voltage, which is then amplified by an amplifier and is fed back to an analog-digital converter (ADC) integrated into the microcomputer. The microcomputer adjusts its command value to the linear IPS in response to the feedback signal. This system allows accurate current to flow to the load (solenoid valve).

Fuji Electric's conventional linear IPS is a power IC that integrates a power MOSFET for current control, a control unit, and an amplifier for current detec-

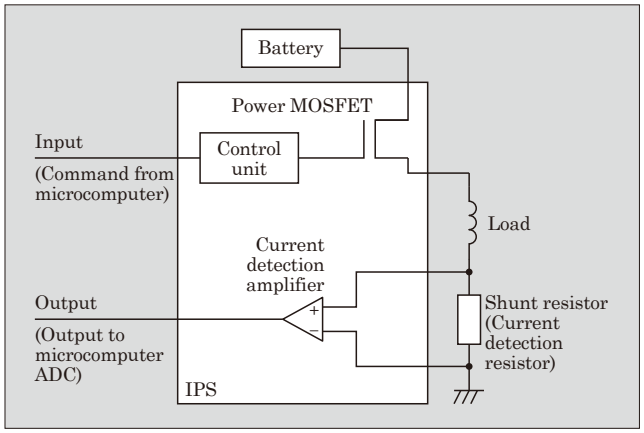


Fig.1 Conventional linear IPS usage

tion into a single chip as shown in Fig. 1, contributing to high-density mounting on ECU boards. To detect the current flowing through the load accurately, the current sensing amplifier has the circuit and layout design that is optimized to minimize the error generated in the output voltage.

### 2.2 Challenges related to single-chip integration

The greatest need for the linear IPS is to facilitate the miniaturization of ECU boards. Therefore, in order to achieve further miniaturization, we studied the integration of a shunt resistor in the linear IPS.

The biggest challenge when integrating shunt resistors is heat generation. If a resistor with the same resistance values as those of ECUs currently used in the market was incorporated in the chip, there would be a problem of excessive chip temperature rise due to Joule heat generated by the resistance. Considering the heat dissipation of the package, it is necessary to reduce the resistance value to one-fourth of the present value in order to integrate a shunt resistor into the chip. When the resistance is reduced to one-fourth, the input voltage of the amplifier is also reduced to one-fourth. Therefore, to maintain the input current-amplifier output voltage characteristic, the differential gain of the amplifier must be increased to 4 times the conventional gain (see Figs. 2 and 3).

By increasing the differential gain by a factor of 4, the input-output characteristic can be maintained, but at the same time, there is a disadvantage of increasing the error generated in the output voltage.

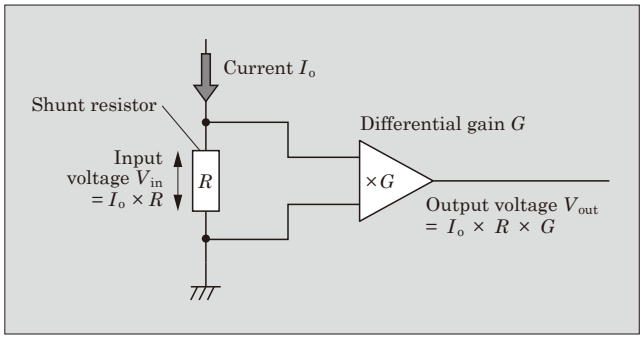


Fig.2 Shunt resistor and output voltage (conventional product)

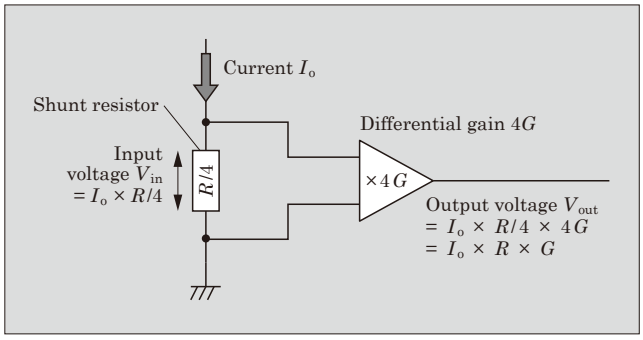


Fig.3 Shunt resistor and output voltage (newly developed product)

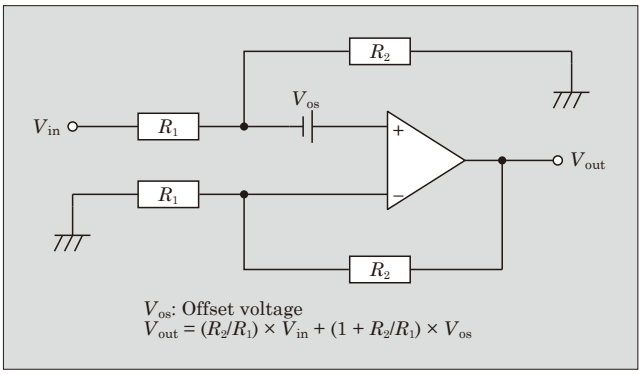


Fig.4 Differential amplifier circuit diagram

Figure 4 shows the circuit diagram of a differential amplifier using OP amplifiers with an offset voltage. The offset voltage is the error in the DC voltage generated at the input of the OP amplifiers. The error is caused by the difference between the threshold voltages of two paired transistors, called a differential pair, due to manufacturing variations. In the differential amplifier circuit shown in Fig. 4, denoting the input voltage as $V_{in}$, the output voltage as $V_{out}$, and the offset voltage as $V_{os}$, then the output voltage $V_{out}$ is given by Equation (1).

$$V_{out} = (R_2/R_1) \times V_{in} + (1 + R_2/R_1) \times V_{os} \quad \cdots\cdots\cdots (1)$$

$V_{in}$ : Input voltage
$V_{out}$: Output voltage
$V_{os}$ : Offset voltage

Here, $(R_2/R_1) \times V_{in}$ is the magnitude of the signal and $(1 + R_2/R_1) \times V_{os}$ is the error due to offset voltage. Applying Equation (1) to Fig. 2, we obtain Equation (2), since $R_2/R_1$ corresponds to the differential gain $G$ and $V_{in}$ corresponds to the input current $I_o \times R$.

$$V_{out} = G \times I_o \times R + (1 + G) \times V_{os} \quad \cdots\cdots\cdots\cdots\cdots (2)$$

$V_{out}$: Output voltage
$V_{os}$ : Offset voltage
$G$ : Differential gain
$I_o$ : Input current
$R$ : Shunt resistor

On the other hand, in Fig. 3, the output voltage is expressed by Equation (3).

$$V_{out} = 4\,G \times I_o \times R/4 + (1 + 4\,G) \times V_{os}$$
$$= G \times I_o \times R + (1 + 4\,G) \times V_{os} \quad \cdots\cdots\cdots\cdots\cdots (3)$$

Comparing Equations (2) and (3), the magnitude of the signal remains unchanged at $G \times I_o \times R$, while the error increases from $(1 + G) \times V_{os}$ to $(1 + 4\,G) \times V_{os}$. For example, if the differential gain $G$ increases by a factor of 8, the error generated in the output voltage increases by a factor of approximately 4, from 9 $V_{os}$ to 33 $V_{os}$.

Thus, integrating a shunt resistor allows the ECU board to be smaller but has the detrimental effect of increasing the error in the output voltage of the differ-

ential amplifier. To solve this problem, it is necessary to reduce the offset voltage of the OP amplifiers that comprise the differential amplifier.

Techniques to reduce the offset voltage include optimizing device layout on the chip and trimming during shipping tests. However, the effect of optimizing device layout is limited. In addition, it is difficult to compensate for offset voltage fluctuations due to temperature changes after adjustment when trimming during shipping tests. In light of this, we have developed and applied an auto-zero amplifier technology that self-compensates for offset voltages at regular intervals.

## 3. Features of Auto-Zero Amplifier Technology

### 3.1 Configuration of the next-generation IPS using an auto-zero amplifier

Figure 5 shows the block diagram of the next-generation IPS. As a countermeasure against the increase in error caused by an integrated shunt resistor, it uses an auto-zero amplifier as the current-sensing amplifier. Element devices include a power MOSFET for current drive, a control unit for controlling the power MOSFET, a shunt resistor, and a 5-V current-sensing amplifier (application of auto-zero amplifier), all on a single chip.

### 3.2 Auto-zero amplifier

(1) Operating principles

Figure 6 shows the operating principle of the auto-zero amplifier.

The auto-zero amplifier consists of two OP amplifiers, namely, a main amplifier and a correction amplifier. Each OP amplifier has an input terminal for offset voltage correction (CO terminals in the figure) in addition to the normal + and – inputs. $V_{os}1$ is the offset voltage of the main amplifier, and $V_{os}2$ is the offset voltage of the correction amplifier.

SW1 and SW2 alternately turn on and off, and SW3 and SW4 also alternately turn on and off. As for the timing of switching, SW1 and SW3 turn on simultaneously and SW2 and SW4 turn on simultaneously. Capacitors C1 and C2 hold the respective correction voltages of the main amplifier and correction amplifier.

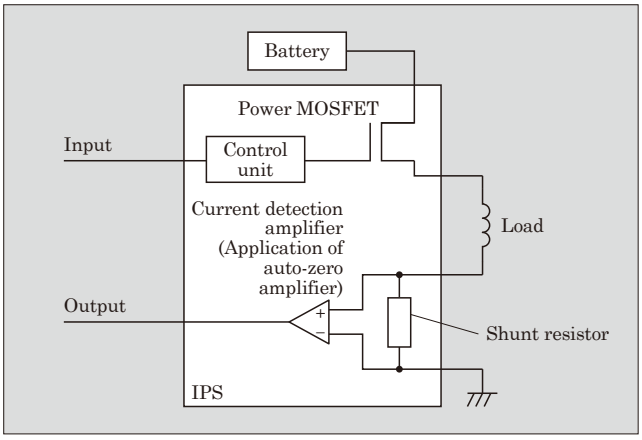


Fig.5 Block diagram of the next-generation IPS

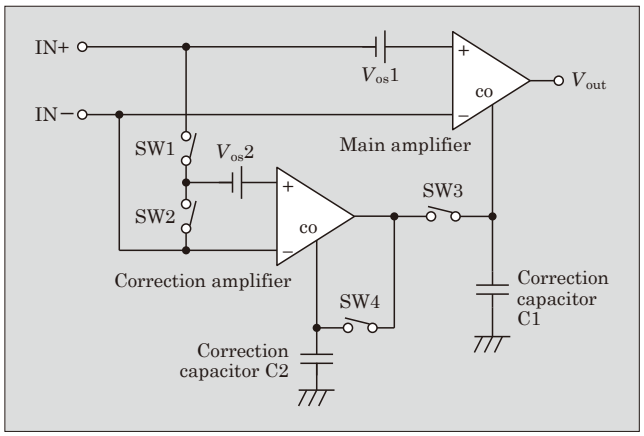


Fig.6 Operating principle of the auto-zero amplifier

The auto-zero amplifier operation is divided into two phases depending on the SW connection status.

(a) Phase 1: SW1 and SW3 = Off; SW2 and SW4 = On

A correction amplifier corrects its own offset voltage. Since both inputs of the correction amplifier are short-circuited, the correction amplifier receives its own offset voltage $V_{os}2$. The output of the correction amplifier is connected to its own correction terminal CO via SW4. Therefore, the correction amplifier outputs a voltage that cancels its own offset voltage $V_{os}2$ and charges the correction capacitor C2.

(b) Phase 2: SW1 and SW3 = On; SW2 and SW4 = Off

Correction is performed for the main amplifier. IN+ is connected to the + terminal of the correction amplifier via its own offset voltage $V_{os}2$, and IN– is connected to the – terminal. $V_{os}2$ is connected to the + terminal of the correction amplifier, but the correction amplifier has already been offset corrected in Phase 1 and no offset voltage component is superimposed on the output.

Since the main amplifier operates with negative feedback, the potentials of the main amplifier's + and – terminals become equal. Therefore, the voltage difference between IN+ and IN– becomes the offset voltage $V_{os}1$ of the main amplifier. The offset voltage $V_{os}1$ of the main amplifier is input to the correction amplifier. The correction amplifier outputs a voltage that cancels the offset voltage $V_{os}1$ of the main amplifier and charges the correction voltage to the correction capacitor C1 of the main amplifier.

By periodically repeating Phases 1 and 2, the correction voltages of the correction amplifier and main amplifier are always kept at the optimum value, minimizing the error generated by the main amplifier output.

(2) Reduction of operating power supply voltage

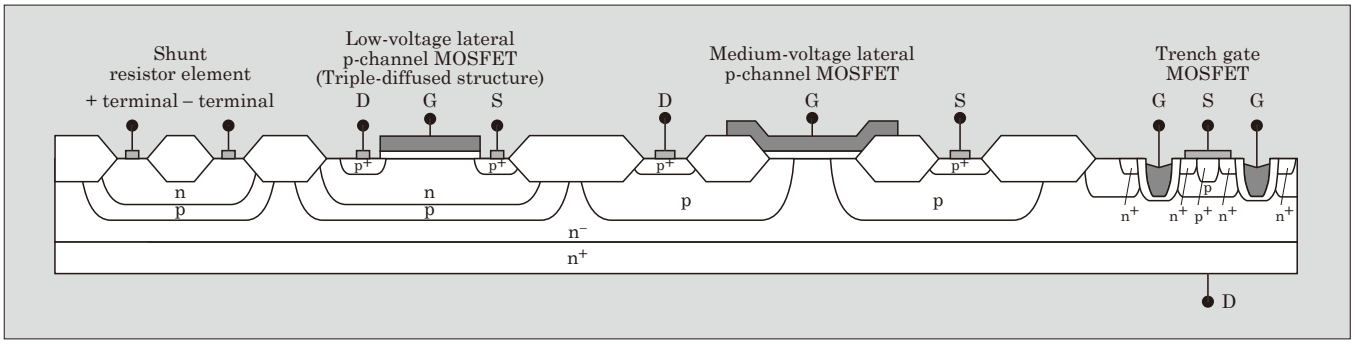


Fig.7 Cross-sectional structure of the 5th-generation IPS device

The next-generation IPS is required to integrate the power MOSFET with 5-V circuit on a single chip, and we have developed the auto-zero amplifier technology using 5th-generation IPS device and processing technology.[5] Figure 7 shows the cross-sectional structure of a device applying the 5th-generation IPS device processing technology. The feature of this process is that a trench gate MOSFET for current drive, a medium-voltage MOSFET, a low-voltage MOSFET with triple-diffused structure, and a shunt resistor can be integrated on a single chip. This makes it possible to achieve auto-zero amplifier technology that automatically corrects the offset voltage while providing the current drive capability and breakdown voltage performance required for automotive power ICs.

In general, a triple-diffused structure requires a high impurity concentration in the topmost layer, and MOSFETs formed in that layer tend to have a high threshold voltage. The same trend was observed for the low-voltage MOSFETs with a triple-diffused structure used in this research. Circuits composed of high-threshold-voltage MOSFETs will have a higher operable power supply voltage. In contrast, the market is requiring power supplies to operate at low voltages to improve tolerance to power supply voltage fluctuations. Therefore, we took the following measures to reduce the operating voltage in our newly designed auto-zero amplifier.

(a) Bias circuit

We have modified the bias circuit, which must start operating at the lowest power supply voltage of the circuits. In particular, we achieved low-voltage operation by changing the circuit configuration in areas with a large number of MOSFET layers and optimizing the bias conditions of the MOSFETs.

(b) Under voltage lockout (UVLO) circuit

The amplifier output becomes undefined when the power supply voltage is low and the operating voltage of the amplifier is not sufficient. Since outputting a signal to the microcomputer's ADC in an undefined state can cause a system malfunction, it is equipped with a UVLO circuit that fixes the amplifier output at 0 V until the amplifier output converges. If the reference voltage that fixes the amplifier at 0 V fluctuates due to manufacturing variations, the guaranteed operating voltage will be higher. Therefore, we have improved the circuit to minimize the effect of manufacturing variations on the reference voltage.

This innovation has made it possible to achieve an operating voltage equivalent to that of conventional products using a triple-diffused structure process.

## 4. Effect of the Auto-Zero Amplifier

Figure 8 shows the evaluation results of an actual device using an auto-zero amplifier. The gain was set to 32 times, four times that of the conventional product, taking into account that the shunt resistance is one-fourth of the conventional resistance. A load current applied to the input of the amplifier was 1 A and the voltage, equivalent to that when using one-fourth of the shunt resistance used for the conventional product. Current detection accuracy was evaluated under these conditions in a temperature range of −40°C to +175°C. The target value was equal to that of the 5th-generation IPS[4].

As shown in Fig. 8, the target specifications of the 5th-generation IPS are satisfied even though the gain is 32 times, which is four times that of the conventional product.

The evaluation results suggest the auto-zero am-

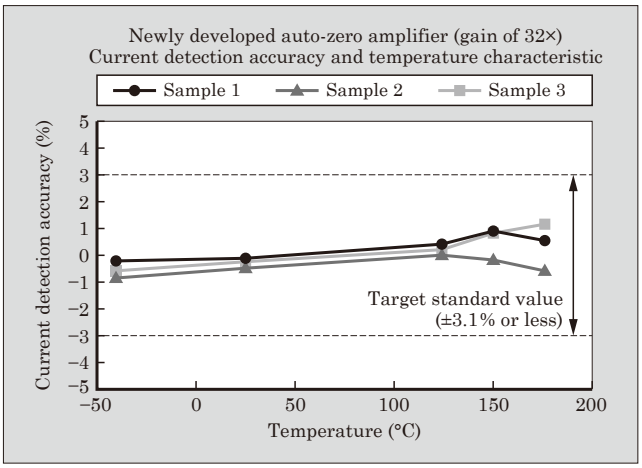


Fig.8 Evaluation results of an actual device using an auto-zero amplifier

plifier technology can solve the increase in error that would otherwise occur when an IPS and shunt resistor are integrated into a single chip. The built-in shunt resistor is expected to reduce the size of the ECU board, and the current detection accuracy is expected to be the same as that of conventional products.

## 5. Postscript

We have developed an auto-zero amplifier technology for IPSs that can be utilized in automotive power ICs. This is expected to reduce the size of the ECU board while maintaining the same level of current detection accuracy as conventional products.

In the automotive field, which is rapidly becoming more electronic, we believe that this technology will be used in a wide range of applications other than IPSs. Going forward, Fuji Electric continues to study ways to expand the scope of application and contribute to the automotive industry.

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