Noise Reduction Methods for Power Electronic Equipment

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1. Introduction

Power electronic equipment represented by such equipment as inverters and servos are used in a wide range of applications from industrial factories to ordinary homes for improving productivity and/or saving energy.

Wider use of these equipment is expected in the future, however there is concern that noise generated by these equipment may adversely influence other equipment.

The noise generated by these equipment can be roughly classified in the following three categories:

① harmonic current emissions flowing into the power source (abbreviated as "source harmonic currents" below),
② disturbance voltages generated from the main source terminals (abbreviated as "main terminal disturbance voltage" below), and
③ electromagnetic interference radiated out of the equipment itself (abbreviated as "electromagnetic disturbance emission" below)

These noise levels are regulated by several guidelines(1).

Several noise reduction methods will be introduced in this paper.

2. Noise Reduction Methods

2.1 Reduction of source harmonic currents

In the main circuits of many power electronic equipment, capacitor-input type diode rectifying circuits are generally used as rectifiers for converting AC voltage to DC voltage. Figure 1 (a) shows a single-phase rectifier circuit. The current from the power source shown in this figure flows through a reactor and a single-phase full-wave rectifier bridge and charges a smoothing capacitor. The current flow and the line terminal voltage are shown in Fig. 1 (b). As the figure illustrates, the waveform of the current flowing in the power source becomes distorted. There are concerns that this distorted current may influence other equipment connected to the same power source resulting in overheating, audio noise, vibration and other disturbances. Therefore, it is necessary to reduce this

Fig.1 Configuration of capacitor input type diode rectifier circuit and its operating waveforms

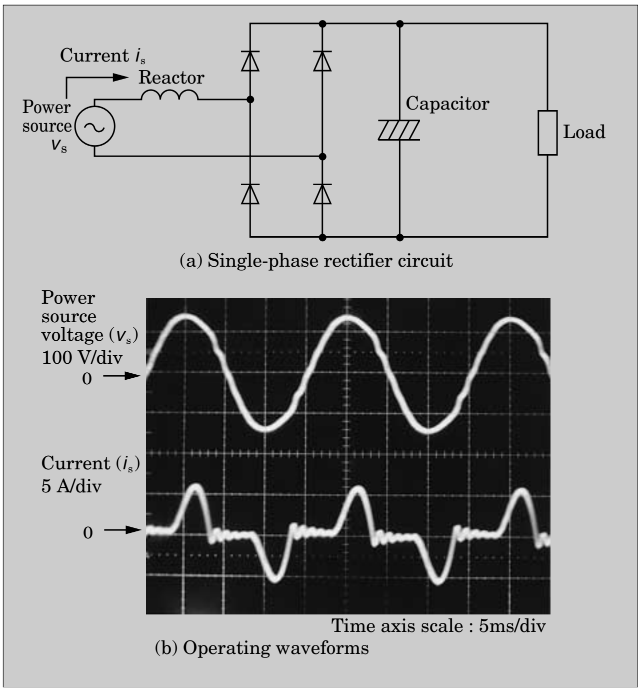
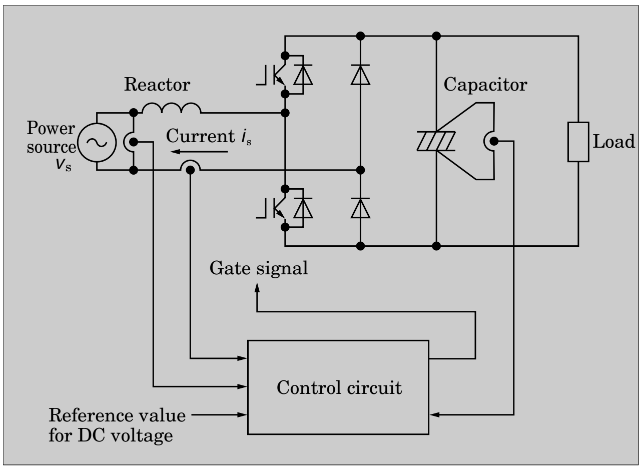


Fig.2 Circuit configuration of single-phase PWM converter with line current sensor



distorted wave current, the so-called source harmonic current. Connection of a reactor and use of a PWM (pulse width modulation) converter are methods to reduce noise.

Figure 2 shows an example of source harmonic currents reduction methods. In this method, because the line current is directly controlled, a line current sensor must be provided and the converter control circuit must be insulated from the current sensor. This increases complexity of the circuit structure and reduces reliability.

A reduction method that suppresses source harmonic currents below a regulated level without using any line current sensor will now be introduced.

The circuit diagram of a line current sensor-less single-phase PWM converter and its operating waveforms are shown in Figs. 3 (a) and (b) respectively. These waveforms illustrate the source harmonic currents clearing the regulated level. An advantage of this method is that insulation from the main circuit is not necessary because the line current sensor is replaced with a DC current sensor.

The operating principle of this line current sensorless single-phase PWM converter is briefly explained below.

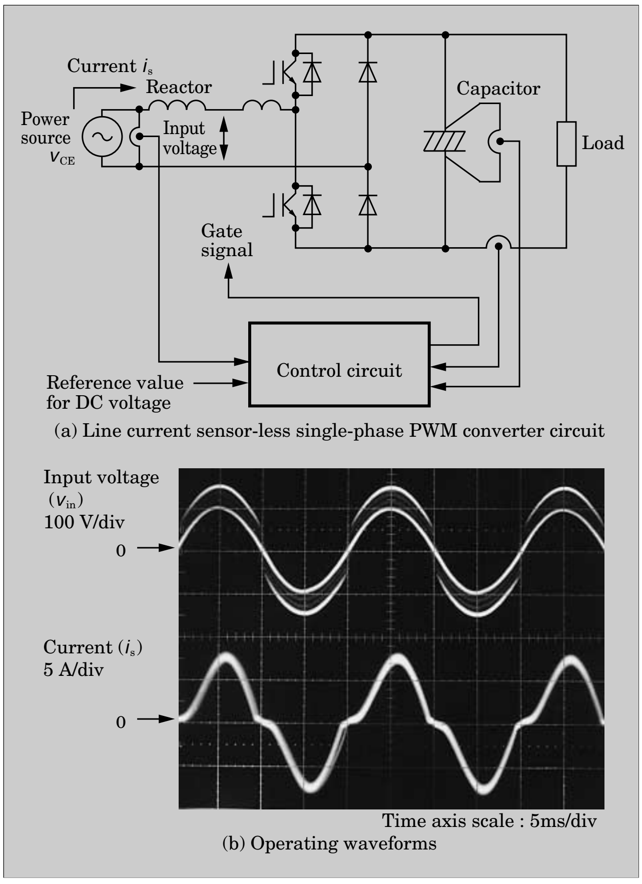
To reduce the source harmonic currents it is appropriate to make a sinusoidal wave current flow in phase with the source line voltage. In other words, the converter must generate a sinusoidal wave voltage, equal to the line voltage plus the reactor voltage drop, at its input terminal. Specifically, a sinusoidal wave voltage for making the source power factor equal to 1 must be calculated from the converter output power and the reactor's reactance. If the converter generates the calculated voltage at its input terminal, the waveform of the line current becomes sinusoidal in steady state.

2.2 Reduction of main terminal disturbance voltages

Main terminal disturbance voltages generated by power electronic equipment are caused by harmonic current flowing from the equipment into the power source due to semiconductor switching devices turning on and off in the main circuit. Details of the mechanism that generates this phenomenon is described in technical reports and other documents. The mechanism will be briefly explained below.

Harmonic currents flow when voltage transitions (abbreviated as "*dv/dt*" below), generated by the on-off of semiconductor switching devices, are added to the stray inductance and stray capacitance of electrical components that comprise the equipment. In other words, these harmonic currents depend on the *dv/dt* of semiconductor switching devices. Therefore if this *dv/dt* is made smaller, the harmonic currents decrease

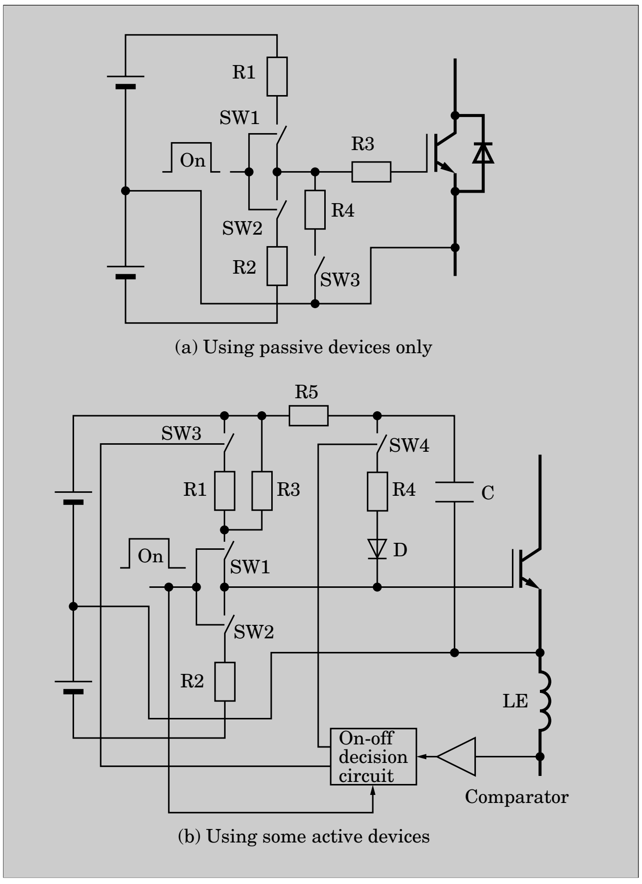
Fig.3 Circuit configuration of line current sensor-less single-phase PWM converter and its operating waveforms



(a) Line current sensor-less single-phase PWM converter circuit

(b) Operating waveforms

Fig.4 Gate driving circuit



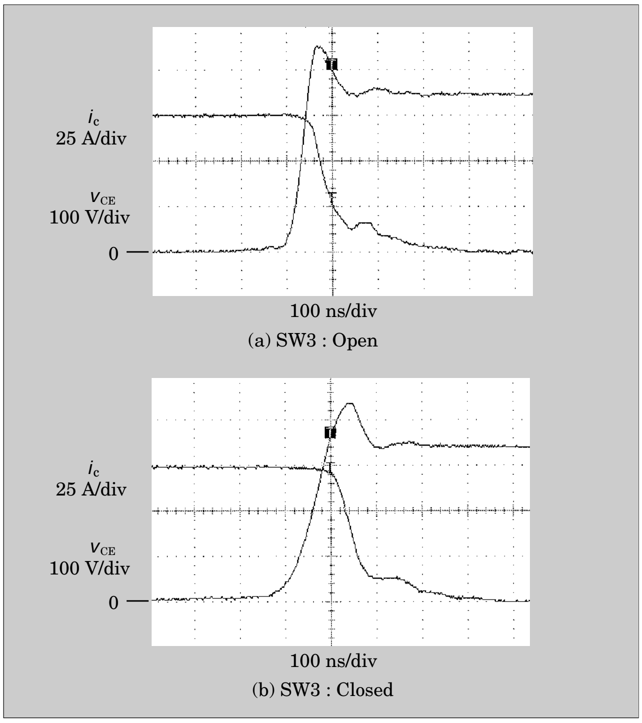
(a) Using passive devices only

(b) Using some active devices

and then the main terminal disturbance voltages can be reduced.

Therefore, *dv/dt* of semiconductor devices used in main circuits, specifically IGBT devices, must be made smaller. A gate driving circuit for smaller *dv/dt* will be introduced below.

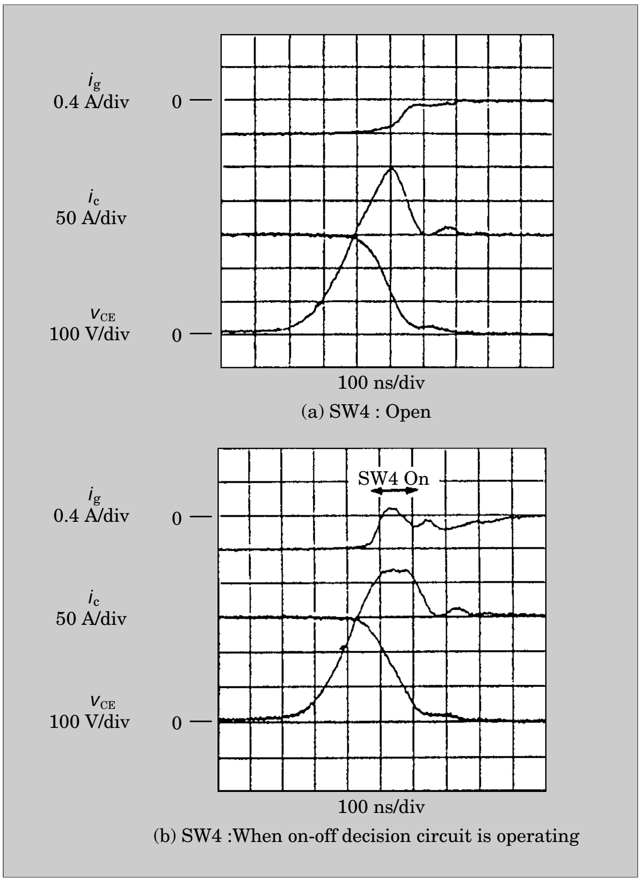
Fig.5 Operating waveforms (device used : 2MBI 75-060N)



(a) SW3 : Open

(b) SW3 : Closed

Fig.6 Operating waveforms (device used : 2MBI 150N-060)



(a) SW4 : Open

(b) SW4 :When on-off decision circuit is operating

Figure 4 (a) shows a gate driving circuit composed of passive devices only and Fig. 4 (b) shows another driving circuit that uses several active devices. Figures 5 and 6 show the operating waveforms at the time of turn-off for the IGBT devices driven by these gate driving circuits. Figure 5 illustrates the difference of *dv/dt* when the gate current value is changed by a switch (SW3) in the circuit configuration of Fig. 4 (a). Figure 6 illustrates the difference of *dv/dt* when switches (SW3, SW4) in the circuit configuration of Fig. 4 (b) are kept open and operated according to the on-off decision circuit. As these operating waveforms show, *dv/dt* can be suppressed by the gate driving conditions. The operation of these driving methods is explained below.

It is known that the *dv/dt* of IGBT depends on the value of gate resistance. When the resistance value is increased, the *dv/dt* generally tends to decrease. This characteristic can be utilized to suppress the *dv/dt*. The circuit in Fig. 4 (a) is configured to drive the gate after the gate resistance value has been changed externally by switch SW3. An advantage of this method is that the gate current level can be changed by switching switch SW3 and thus the gate driving circuit consists of fewer parts. On the other hand, although the *dv/dt* itself can be made smaller, this method has a disadvantage in that a smaller *dv/dt* makes the switching power loss larger. This method may be utilized in applications that allow a reduced number of switching times (frequency) for suppressing noise generation.

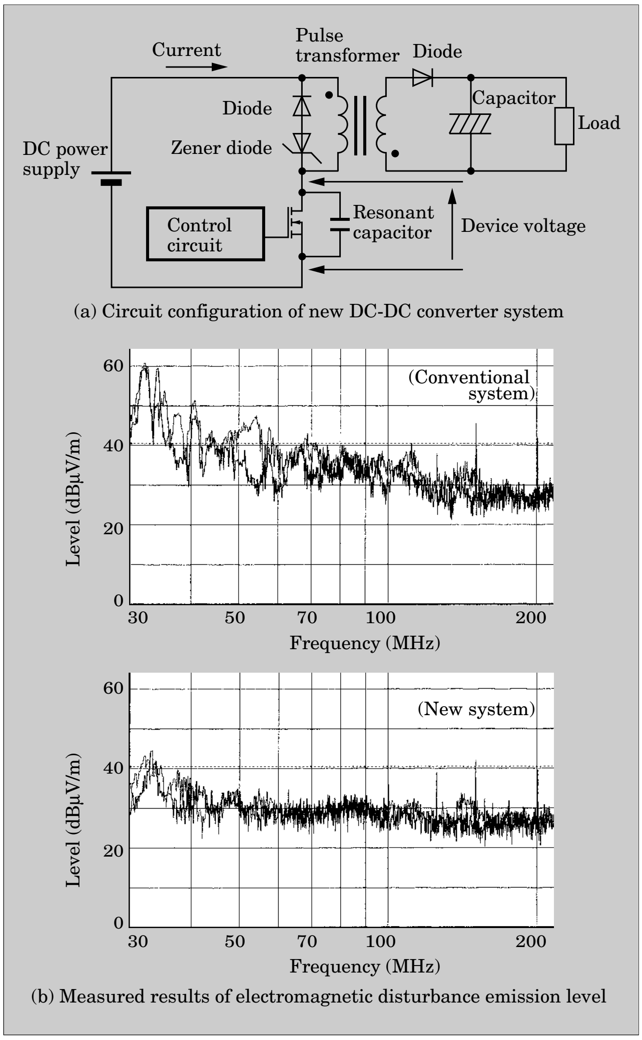
The configuration of the circuit in Fig. 4 (b) is a further development of the above-mentioned method. This method reduces both the *dv/dt* and the switching power loss by detecting current transitions, making good use of wiring stray inductance between IGBT chips in the IGBT module and the module terminal block, and by suppressing the values of gate resistance and voltage at on-off time points.

2.3 Reduction of electromagnetic disturbance emission

In the same manner as main terminal disturbance voltages, electromagnetic disturbance emission generated by power electronic equipment is caused by harmonic currents flowing from an equipment into the power source. However, the electromagnetic disturbance emission has a higher frequency range than main terminal disturbance voltages and is emitted from the equipment in the form of electromagnetic waves. Details of this mechanism are described in technical reports and other documents.

The main source of electromagnetic disturbance emission from inverters or servo-amplifiers is semiconductor switching devices that are used in the main circuits and switching regulator type power supplies in

Fig.7 Configuration of DC-DC converter circuit and measured results of electromagnetic disturbance emission level

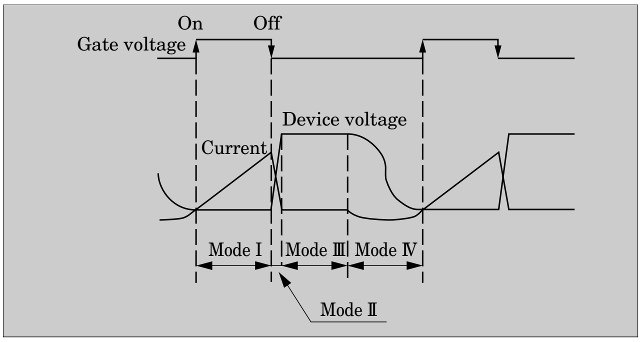


(a) Circuit configuration of new DC-DC converter system

(b) Measured results of electromagnetic disturbance emission level

control circuitry for power electronic equipment. The electromagnetic disturbance emission is generated when such devices switch on and off. The method of reducing noise from the former main circuit has already been described in section 2.2. The method for reducing noise from the latter switching regulator will be described below. For cost-performance considerations, a fly-back type DC-DC converter (abbreviated as “DC-DC converter” below) is generally utilized as the switching regulator. To lower the emission of electromagnetic disturbance emission from the DC-DC converter, it is sufficient to reduce the *dv/dt* of the main switch. The main switch is most commonly a device such as an IGBT or MOSFET. To reduce *dv/dt* of the device, as described in the previous section, it is effective to increase the value of gate resistance. However, it is anticipated that this would increase the switching power loss and thus lower efficiency and require larger cooling fins for the devices. Further, the longer switching time makes high frequency switching difficult. As a result, the size of a pulse transformer used in the DC-DC converter will become larger.

Fig.8 Operation timing-chart (new system)



Here a new DC-DC converter system utilizing resonance phenomena will be introduced. Figure 7 (a) shows the circuit structure of the new DC-DC converter system and Fig. 7 (b) shows measured levels of the electromagnetic disturbance emission from a certain conventional system and the new system. As Fig. 7 (b) illustrates, the new system radiates less electromagnetic waves by approximately 15 dB (at nearby 35 MHz). The operating principle of the new DC-DC converter system will be briefly explained below.

Figure 8 shows a timing-chart of operation of the new system. In this figure, after resetting the pulse transformer (mode Ⅲ), a resonance phenomenon occurs between the primary inductance of the pulse transformer and the resonant capacitor (mode Ⅳ). The device voltage drops according to a certain *dv/dt* determined by the resonance phenomena. If the device is turned on at the lowest point of the phenomena, the *dv/dt* of the device at its turn-on time point can be made smaller than the case where resonance phenomena is not utilized. In theory, no switching power loss is produced due to zero voltage switching. Because the resonant capacitor acts as a snubber, the *dv/dt* of the device at the turn-off time point can be reduced. Further, the switching power loss becomes theoretically zero because the device current commutes to the snubber at that time. Therefore, it is possible to reduce the *dv/dt* without increasing switching power dissipation.

3. Conclusion

Several noise reduction methods for power electronic equipment represented by power converters have been introduced above. In the future, such equipment may come into wider use throughout the world and accordingly various regulations regarding noise will be enforced further.

Fuji Electric will continue to promote the timely research and development of noise reduction techniques to meet market requirements.

Reference

(1) CISPR Pub.11 (CISPR : Comité International Social des Perturbations Radio-electriques) (1990)