UDC 621.382.049.774

PRESENT STATUS AND PROSPECTS FOR FUJI ELECTRIC'S IC TECHNOLOGY

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1. FOREWORD

With the increasing expansion and advance of the functions of various electronic apparatus and systems, higher integration density and multiple functions are being demanded of IC. Then, the advance of IC technology is also exceeding the past trend, especially for fine processing, and many problems are being solved. There is the advance also in the custom IC field aimed at by Fuji Electric.

Up to now, Fuji Electric tackled the high market growth information equipment with miniaturization and advancement of the functions, and personalization of the terminal equipment and also planned development to automatic focusing camera, CPU equipment, etc. And technology has advanced positively by structure design for high voltage, process design for multiple functions, etc. to meet the demands of users at that process.

The present status, features, and prospects of Fuji Electric's IC technology are outlined below.

2. PRESENT STATUS OF FUJI ELECTRIC'S IC TECHNOLOGY

Since the main objective of Fuji Electric's IC technology up to now was the high power functional segment and control peripherals of IC for various information equipment, it featured:

(1) High voltage, high current
(2) Analog-digital mixed mode and sensor, logic circuit integration for multiple functions
(3) Bump electrode for high density assembling

To obtain these features, various innovations are introduced into the device structure, process, and assembling.

Taking the operating voltage as an example, whereas low power consumption CMOSIC usually operate at 5V, the Fuji Electric CMOSIC can operate at 40V and capacities over this can be handled with DMOS (Double Diffused MOS) IC technology.

The output current per unit area versus output voltage is shown in *Fig. 1*. In other words, the suitable IC technology spacing a wide output voltage range from 4V to 500V can be selected according to the required functions.

Next, the technologies related to the wafer fabrication

Fig. 1 Output current per unit area versus output voltage

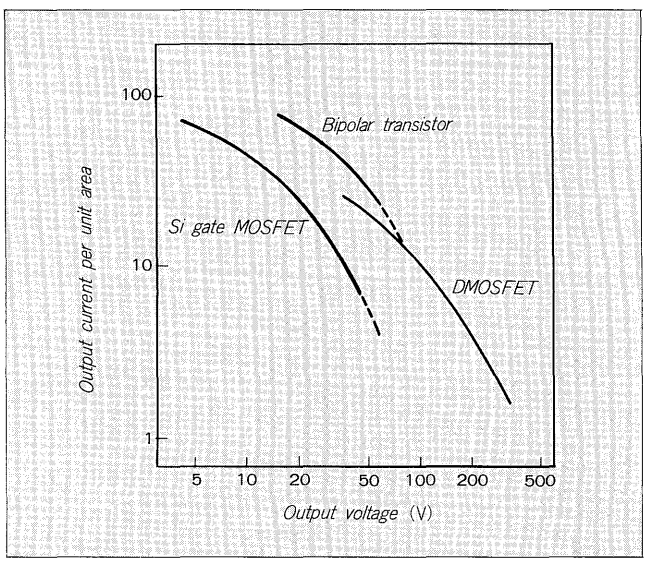
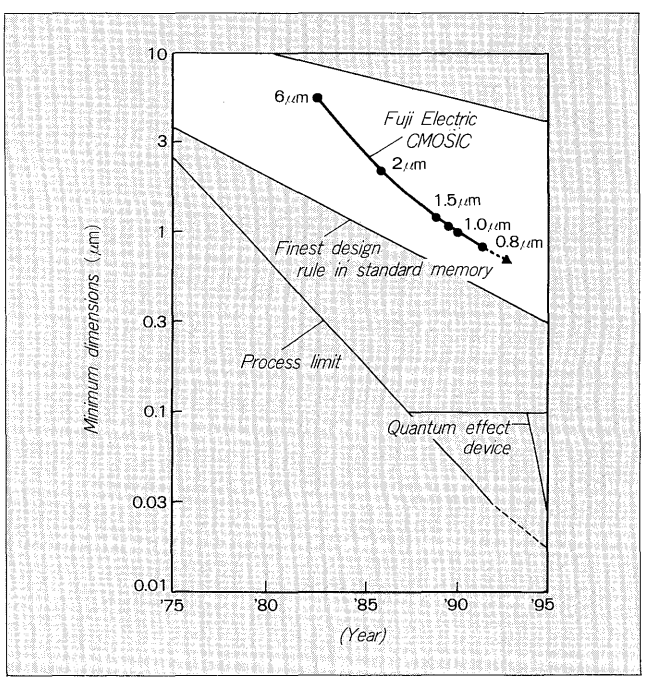


Fig. 2 Progress of design rule in LSI



and their application products will be discussed.

2.1 Process technology

Regarding the fine process which is the foundation of process technology, up to now, the DRAM has become the leading device and the process is being improved. However, from the standpoints of increasing the number of transistors integrated on one chip, cost competition, even in the custom IC field, fine processification is advancing and the difference in design rule from DRAM is decreasing.

The progress of design rule in LSI at Fuji Electric is shown in *Fig. 2*. These values are for the gate length on the photo mask.

Fuji Electric's process technology consists of the four type shown below. These technologies are used according to the functions required.

(1) Si gate CMOS
(2) Bipolar linear
(3) Bi-CMOS
(4) DMOS

The main specifications and features of these are shown in *Table 1*. Of these, Si gate CMOS technology is, of course, applied to logic and other low voltage segments and is also applied to LCD panel, thermal head drive and other high voltage output segments with operating voltages up to about 40V. To high voltage output segments, normally, 4μm design rule is applied and high voltage design is performed.

For bipolar linear technology, the main objectives are automobile ignitor, regulator, sensor, and various power source DC-DC converters, and line operation and high integration, high voltage is featured.

Bi-CMOS technology is mainly applied to analog-digital mixed mode microcomputer interfaces, sensors, etc. and high integration is realized by fine processification, single-poly, double-metal layer metallization, etc.

DMOS technology allows operating voltages up to 500V and devices and processes which can easily combine the CMOS, bipolar, and DMOS processes are designed. Up to now, it has been applied to plasma displays and VFD panels.

2.2 High density assembly

To meet the trend toward small and flat electronic apparatus, the demand for high density assembly is also strong. To meet this demand, the use of the bare chips method without package is increasing, with information equipment as the main objective. In the past, Fuji Electric featured the bump electrode IC for TAB and flip chip bonding. The TAB and flip chip bonding method have such advantages as reduction of the assembly process and for multiple pin chips, a substantial reduction of the chip size compared to wire bonding and improvement of the assembling density for multiple chips. The Fuji Electric assembling technology is outlined in *Table 2*.

Namely, besides wire bonding, there is TAB and flip chip bonding. Among them, with the TAB method, gold bump is used and a bump shape of an appropriate size

Table 1 Fuji Electric's process technology

Process technology	Main specifications	Features	Application objective examples
Si gate CMOS	Operating voltage 4~40V Operating frequency 50MHz	High voltage structure possible	LCD panel Custom memory
Bipolar linear	Operating voltage 5~24V Cut-off frequency 2GHz	High integration density High voltage	Automobile Various power sources
Bi-CMOS	Operating voltage 5~24V Cut-off frequency 2GHz	High voltage Double layer metallization	Disk drive, sensor Microcomputer interface
DMOS	Operating voltage ~500V Operating frequency 16MHz	High integration density, high voltage Combination of CMOS, bipolar, and DMOS technologies is easy	PDP, EL panel High voltage interface

Table 2 Fuji Electric's assembling technology

Bonding method	Main specifications, etc.					Features	Application objective example
	Electrode size (μm)	Electrode height (μm)	Electrode pitch (μm)	Bonding strength (g/point)	Number of electrodes		
Wire	≧70□	–	≧110	5~10	~208	Conform to EIAJ integrated circuit outline dimensions rules	IC general
TAB (gold bump)	30□~175x75	10~50	60~115	10~20	32~400	High precision, high reliability Bump shape can be selected	Thermal head, various displays
Flip chip (solder bump)	80~160φ	60~150	180~450	20~50	8~160	High bump strength, high reliability Solder composition can be freely selected	Thermal head, LCD, automobile

can be selected from a range of 30μm square or greater according to the required function. The flip chip method is mainly oriented toward the automotive field and uses a solder bump and the solder composition can be selected according to uses.

Both the gold bump and solder bump feature high bonding strength and high reliability.

2.3 Fuji Electric IC

The main specifications, functions, and features for each field of the application objectives of the technologies above are shown in *Table 3*.

Thermal heads and displays are the main objective of the high voltage and high current features by Fuji Electric's IC technology. For autofocus IC, to make sensor, A-D converter and logic circuit a single-chip, much consideration is given to process design, as well as to system, circuit, and device design. Bipolar linear technology is mainly used for power sources and automobiles. The features are FET direct drive and use of a multiple function 8-pin SOP package for power supplies and high accuracy and high reliability for automobiles. CPU peripherals are systems that use Fuji Electric's original CPU core and meet the trend of advanced functionalization and miniaturization of electronic apparatus.

3. PROSPECTS

IC technology, including fine process, is driven by the DRAM and there is no telling when its growth will stop. The functions of custom IC are also rapidly becoming more complex and enhanced with the advance of CAD technology.

From such a background, even in the full custom field aimed at by Fuji Electric, we feel that high density integration and multiple functionalization will be spurred on further because of the demand for increase of additional value and discrimination from competing products by the user and miniaturization and weight reduction, etc.

Therefore, from the standpoint of system structure, the introduction of the advanced function CPU core and

Fig. 3 Development of assembling technology

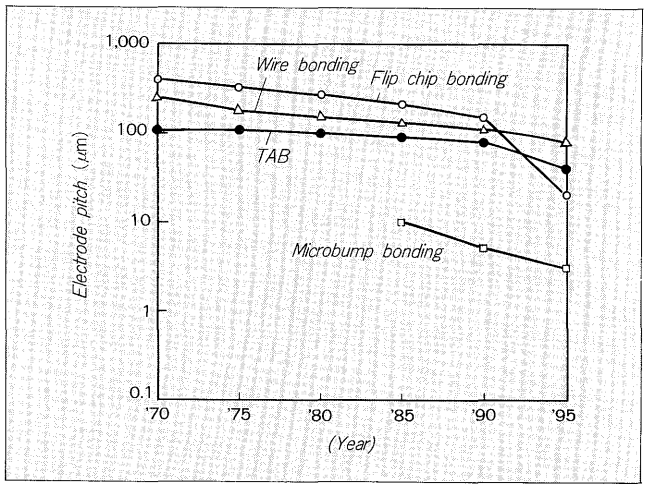
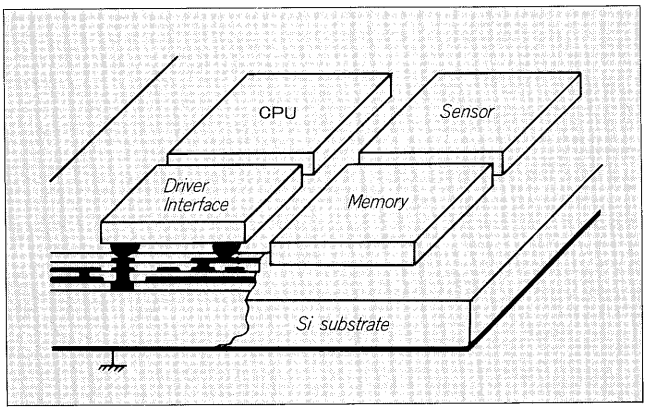


Table 3 Fuji Electric IC

Application objective		Main specifications, functions, etc.	Features
Thermal head driver		Power source voltage 5V Output current 10~80mA Number of outputs 64~192 Mainly gold bump, solder bump	Small chip size by optimum design of output section, Multiple output High density assembly possible by microbump method
Display	LCD	Power source voltage 5V Output voltage 15~40V Number of outputs 50~160 Mainly gold pump	Usable with large panels (active method, 1/480 duty) Multiple output, high voltage Small chip size
	PDP	Power source voltage 5V Output voltage 120~180V Number of outputs 40~80	Both AC and DC systems possible Usable with color panels Small chip size
LED array		Power source voltage 5V Number of outputs 64	Constant current drive
Auto focusing camera		Power source voltage 2.5~6V Phase difference output Integer part 4~6 bits Fraction part 6 bits Output response time 1.2~2ms (0 EV)	Passive method Single-chipping of sensor, A-D converter, and logic circuits Mainly clear mold package
Power source		Power source voltage 1.4~30V DC-DC converter Line operation (improvement of power factor)	FET direct-drive Multiple functions 8-pin SOP package, etc.
Automobile		Ignitor, regulator, acceleration sensor, etc.	High accuracy, high reliability
CPU peripherals		Power source voltage 5V Various displays, vending machine, etc.	Integration of CPU and panel control Parallel interface extension, etc.
Tone modulation		Power source voltage 5V Tone generation time 2.8~20s	Cascade connection possible ROM division possible (~64 segments) Automatic power off possible
Others		Image sensor, proximity switch, timer, etc.	High precision, small output fluctuation, etc.

Fig. 4 High density assembly chip with bump electrode application



integration of the power device, sensor, display device, control and driving blocks and regarding wafer process technology, fine process same order in standard memory, device isolation by wafer direct-bonding method making integration of high voltage and high output segments easy, matching with power device technology, chip multidimensionalization, etc. will develop further. The advance of multi-chip integration technology, etc. are also indispensable for high density packing.

The development of assembly technology is shown in *Fig. 3* and an example of high density assembly chip with bump electrode application is shown in *Fig. 4*. With the microbump method, it will be possible to reach a pin pitch of 3μm or less in the near future. Fuji Electric wants to meet this trend by incorporating the power device technology, etc. with which we have had much experience in the past, in addition to the high voltage, high output, composite functions, bump electrode forming, and other technology which were featured in the past.

4. SUMMARY

The present status and prospects of Fuji Electric's IC technology have been outlined, but there are many aspects of product development in which the user cooperates. We hope that an understanding of the contents of this special issue will assist you in developing more satisfying products.