Scalable Multi-Controller of MICREX-SX Series

Tetsuhito Watanabe
Yoshisada Sakamoto
Yasushi Ishii

1. Introduction

The programmable controller (PLC), a core component of system control, supports total factory automation (FA), has rapidly progressed in response to the needs for diversification and sophistication of FA systems, and demands for downsizing and cost reduction. In recent years, many companies have been competing to realize the new market demands of open architecture products. As the first supplier in Japan, Fuji Electric launched the "MICREX-SX series" that supports a programming language in compliance with the IEC standard (hereafter referred to as the IEC language), IEC 61131-3 (the former IEC1131-3). This support results in program compatibility between PLCs of different manufacturers, increasing flexibility for PLC users. Conformance with several safety standards including the IEC standards and compatibility with open networks has been achieved. Regarding the performance of this scalable multi-controller, sequential instructions have been executed at a rate of 20ns per instruction, the highest speed level at present.

This paper describes the specifications and features of the scalable multi-controller SPH (hardware PLC), the core of the integrated controller MICREX-SX series for open-architectures.

2. System Structure and Outline of the Scalable Multi-Controller

Figure 1 shows the system configuration of the scalable multi-controller SPH. The SPH offers two models of CPU modules. One model is the SPH300 that processes single instructions within an execution time of 20ns (max.), and the other model is the SPH200 that processes single instructions in 70ns.

By installing function software modules in these CPU modules, they can perform functions that were previously executed by function hardware modules such as simplified positioning control or general-purpose communication.

Modules for PIOs or communication are connected via the SX bus. In addition to the power supply module and the baseboard, a maximum of 254 units can be connected. Each module is equipped with LSIs to achieve high-speed data transfer with the SX bus. The SX bus system assures the periodicity of I/O refresh with a minimum setting of 0.5ms. Therefore, the fluctuation of I/O refresh time for each program scan, a frequent user complaint, can be controlled to improve the ease of use.

One system can be constructed from a maximum of 8 CPU modules to form a multi-CPU system. Parallel execution by multiple CPU modules reduces the load of each CPU, and rapidly processes large-scale application programs. Moreover, the CPU module can distribute the load by assigning specific functions to each CPU. The periodicity of I/O refresh is also assured in multi-CPU systems. If ultra high-speed data reception and transfer is required, a multi-CPU system with even higher performance can be constructed with use of the processor bus, a dedicated bus for use by the multiple CPUs. When constructing a multi-CPU system, each module connected to the SX bus or the processor bus can be used by each CPU module as a shared resource.

For communication modules, the SX bus allows for connection of up to 8 remote I/O master modules and up to 16 PC-card interface modules or general-purpose communication modules. In these communication modules, open-network compatible modules are provided for the upper level network of PLCs or for a network between PLCs such as an Ethernet*, and are also provided for the lower level network of PLCs, such as JPCN-1, Device Net and AS-i, to enable connections between different equipment or manufacturers.

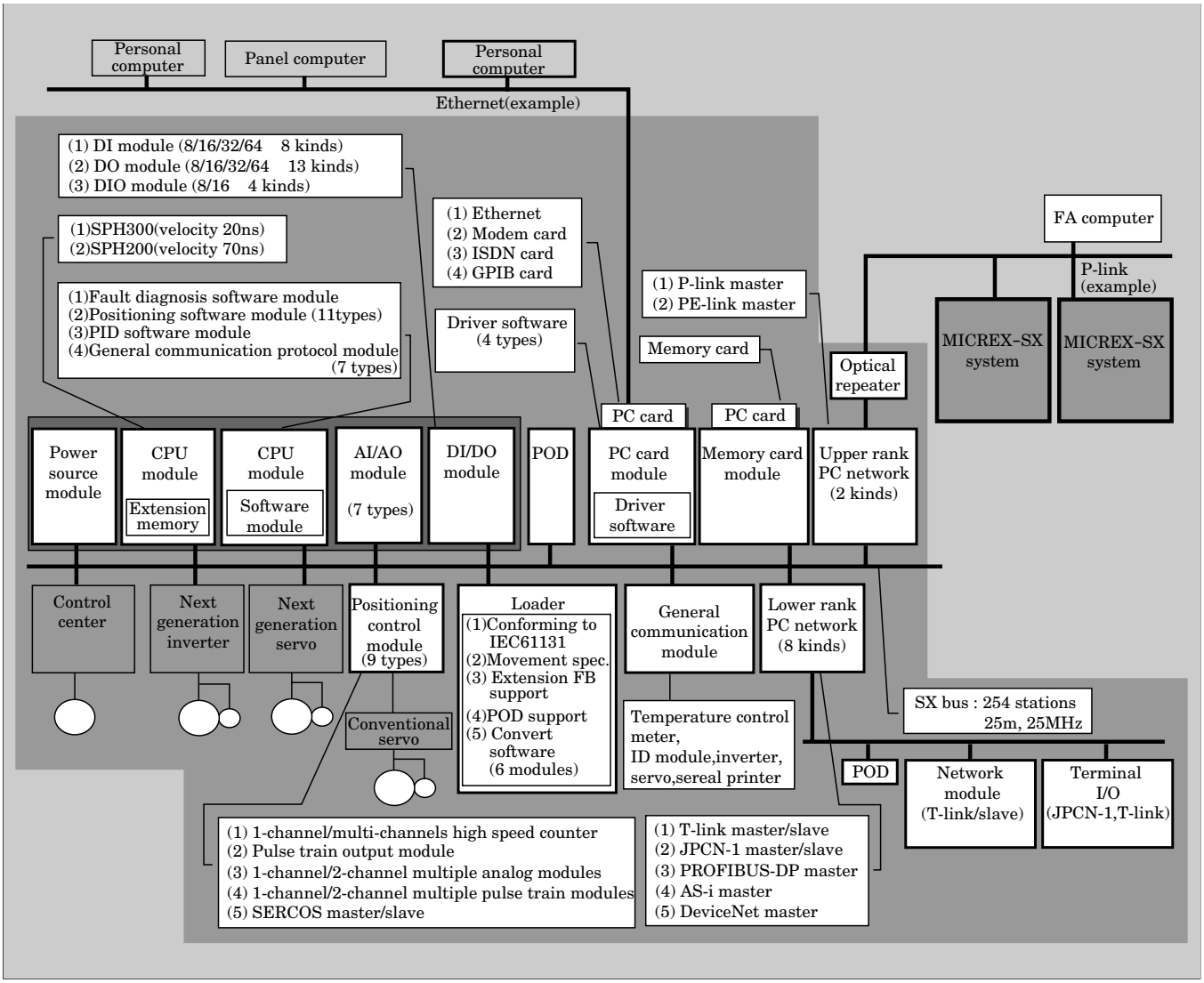
A summary of the basic modules is presented below.

3. The CPU Module

The CPU module of the SPH executes application programs in the IEC language to arithmetically manipulate data that was input from a process, and to output the result to the process. At the same time, the CPU

* Ethernet: A registered trademark of Xerox Corp., USA

Fig.1 System configuration of the scalable multi-controller SPH



module controls initializing, status monitoring, I/O data transfer of the process and message transfer of the overall system (the system bus and various modules of the system components).

3.1 Hardware

Figure 2 shows the printed circuit boards (two-layer construction) of the SPH300. The main technical subjects in developing CPU modules are high-speed, downsizing, cost reduction, low power consumption and measures to prevent noises. The following measures are adopted to solve these subjects.

(1) Development of a LSI processor for IEC language

An intermediate language (referred to as I-code) suitable for RISC architecture has been developed to handle interfaces with program engineering tools. A LSI device (SPH300) with approximately 500k gates contains various custom operators and peripheral control circuits capable of executing a basic instruction in 20ns and a floating-point instruction in 80ns.

Fig.2 SPH300 printed circuit boards

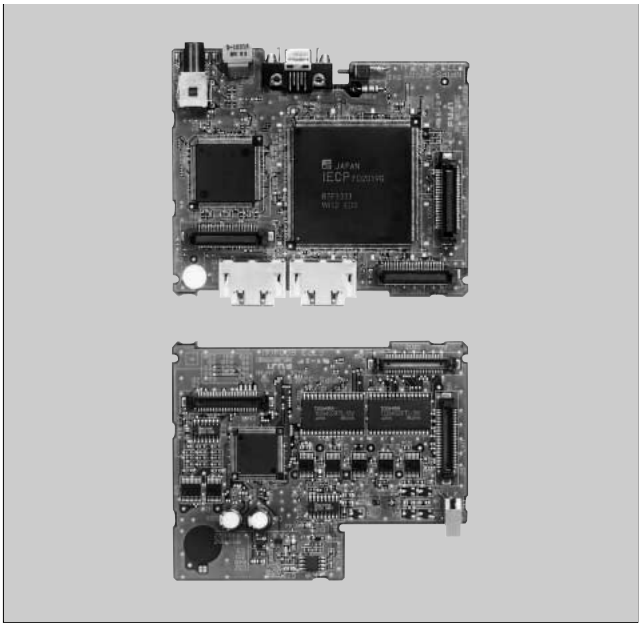


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Table 1 Functions and specifications of the CPU modules for the scalable multi-controller SPH

Parameter		Specifications	
		SPH300	SPH200
Control system		Stored program	
Input/Output connection method		Direct Input/Output method (SX bus), Remote Input/Output method (T-link/JPCN-1)	
Input/Output system		Via SX bus : synchronous refresh Via T-link : 10ms periodic refresh (asynchronous with scan)	
No. of Input/Output points		512 words (maximum 8,192 points)	
CPU		32-bit OS processor 32-bit execution processor	Original processor
Memory capacity	Program	32,768 steps	16,384 steps
	Data	32,768 words	16,384 words
Programming language (In conformity with IEC 61131-3)		IL (instruction list), ST (structured text) LD (ladder diagram), FBD (function block diagram) SFC (sequential function chart)	
Length of instruction		Variable length (depending on language)	
Instruction execution time	Sequential instruction	20ns/instruction or more	70ns/instruction or more
	Applied instruction	40ns/instruction or more	140ns/instruction or more
Data memory	Input/Output memory (IQ)	512 words	
	Instance memory for system FB (SFM)	16,384 words (default value) Timer: 512 points (4,096 words) Integrated Timer: 128 points (1,024 words) Counter: 256 points (1,024 words) Differentiation: 1,024 points (2,048 words) Others: 8,192 words	4,096 words (default value) Timer: 128 points (1,024 words) Integrated Timer: 32 points (256 words) Counter: 64 points (256 words) Differentiation: 256 points (512 words) Others: 2,048 words
	Standard memory (M)	8,192 words (default value)	4,096 words (default value)
	Retain memory (RM)	4,096 words (default value)	2,048 words (default value)
	Instance memory for user FB (FM)	4,096 words (default value)	2,048 words (default value)
	System memory (SM)	512 words	
Available data types		1 bit : BOOL 16 bits : INT, UINT, WORD 32 bits: DINT, UDINT, REAL, TIME, DATE, TOD, DT, DWORD Others: STRING	
Types of tasks	Default task	Cyclic scanning	
	Periodical task	Settled cycle (0.5ms, 1ms to 10s), Task priority : 0 to 3 levels possible	
	Event task	Whenever the assigned BOOL variable changes to “true”, it is executed once. Task priority : 0 to 3 levels possible	
No. of tasks		1 (default) + 4 (sum of periodic task and event task)	
Task priority		0 > 1 > 2 > 3 > default	
No. of POUs	No. of programs	128	64
	No. of function blocks	512	256
	No. of functions	512	128
Diagnostic function		Self diagnostics (memory checking, CPU diagnosis) System structure monitor, System structure module fault monitor	
Calendar function		Time range: until 23:59:59, December 31, 2069	
Backup of memory	Type of battery used	Lithium battery	
	Back up time	5 years (at 25 °C)	

(2) Use of single power supply IC (3.3V)

To realize high-speed control, that is, high-speed operation and a 1ms scan, a single power supply IC (3.3V) is used for all parts, resulting in low power consumption.

(3) 6-layer blind-via-printed circuit board

On printed circuit boards that processes high-speed digital signals, a distributed-constant circuit is formed along the wiring, creating complicated noises.

As a means to prevent noise, a 6-layer blind-via-printed circuit board that connects surface patterns and intermediate layer patterns without boring the front side and back side of the printed circuit boards is utilized to reduce unnecessary inductance along the wiring.

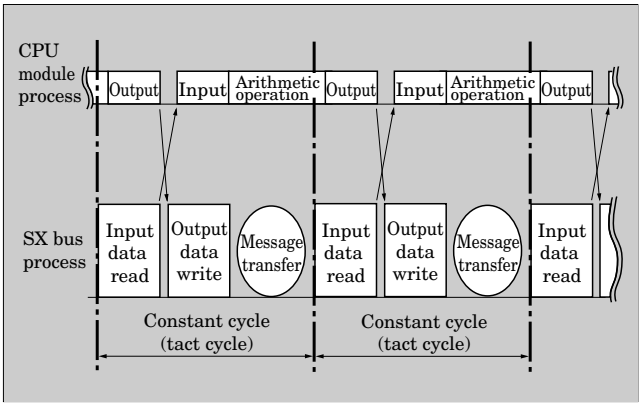
3.2 Functions and specifications

Table 1 lists the functions and specifications of the

Table 2 Basic specifications of the SX bus

Parameter	Specifications
Transmission speed	25Mbit/s
Maximum transmission length	25 m
Number of connectable stations	254 stations (master stations: 8 max.)
Transmission line	Twisted-pair cable (category 5)
Connection type	Bus type (topology: ring type)
Signalizing method	NRZI
Transmission method	Token-pass method and original specifications
Transmission data	Input data Output data Data between processors Message data

Fig.3 Data transfer of the SX bus



CPU modules.

The CPU modules of the SPH have the following features in assigning variables to data memory and task control.

(1) Assignment of data memory

There are two variable areas for the IEC language, one for the I/O data, and another for the memory data. The program is coded by assigning variable names without regard for the physical memory address. There are two data attributes for the memory data area, the initial clear and initial retain.

As shown in Table 1, the CPU module of the SPH divides the data memory into six areas such as I/O memory (IQ), standard memory (M) and retain memory (RM), and assigns these areas corresponding the actual state of the physical memory address that the program engineering tool generates. The "retain memory" is the area where data is saved at initializing.

The size of these memory areas can be changed to comply with various application programs. The system memory that indicates the system status flag and I/O memory are fixed in size.

(2) Task control

Application programs are executed with three types of task scheduling (see Table 1): default tasks, periodic tasks and event tasks. The programs of each task are independently executed in the order of process data input, execution of operation and process data output. The execution is synchronized with data input and output of the SX bus.

3.3 Specifications of language processing

(1) The IEC language and the I-code

When programming with the IEC language in the SPH, the I-code generated by the programming engineering tool corresponds to five types of expressions, making the relevant hardware of the processing system compact. Supported data types are shown in Table 1. In addition to standard functions of the IEC language, extended functions developed originally by Fuji Electric, are also available.

(2) Local variables and global variables

The IEC language supports local variables (variables used in one program) and global variables (variables used by several programs).

In the SPH, access to global variables even with different CPU modules.

4. Bus System

4.1 The SX bus

The SX bus is the system bus at the core of the MICREX-SX Series. Several modules may be distributed in a serial configuration. The SX bus realizes a scalable system structure and has the advantages of smaller size and lower cost compared to conventional parallel buses.

(1) Basic specifications

Table 2 shows the basic specifications of the SX bus. The SX bus has a ring configuration, and can be treated similarly to the bus configuration used to link cable connectors. T-branching is also possible.

(2) Master and slave stations

A maximum of 254 module units can be connected to the SX bus. These modules include master stations and slave stations.

The master station controls the transmission and reception of data, and performs various bus controls and monitoring. The slave station is controlled by the master station, and passively controls the transmission and reception of data for the SX bus.

In a multi-CPU system, a specific master station controls the entire SX bus.

(3) Data transfer cycle

As shown in Fig. 3, data transfer on the SX bus consists of the input data read (status information of each module and process input data), the output data write (process output data) and the message transfer. The data transfer is synchronized with the data input, operation and data output of the CPU module.

The master station controls this data in a transfer tact cycle, that is, in a constant cycle.

Table 3 Summary of I/O module, power supply module and baseboard specifications

Classification	Model code	Outline of specifications	Connection method	Compatibility to standard
Digital input module	NP1X1606-W	24V DC, 16 points, 7mA, variable filter time	Screw terminal	○
	NP1X3206-W	24V DC, 32 points, 4mA, variable filter time	Connector	○
	NP1X6406-W	24V DC, 64 points, 4mA, variable filter time	Connector	○
	NP1X3206-A	24V DC, 32 points, 4mA, variable filter time, internal pulse input	Connector	○
	NP1X0810	100 to 120V AC, 8 points, 10mA	Screw terminal	○
	NP1X1610	100 to 120V AC, 16 points, 10mA	Screw terminal	—
	NP1X0811	200 to 240V AC, 8 points, 10mA	Screw terminal	○
	NP1X3202-W	5V/12V DC, 32 points, 3mA/9mA, variable filter time	Connector	○
Digital output module	NP1Y08T0902	Transistor sink, 12 to 24V DC, 8 points, 2.4A/point, 4A/common	Screw terminal	○
	NP1Y16T09P6	Transistor sink, 12 to 24V DC, 16 points, 0.6A/point, 4A/common	Screw terminal	○
	NP1Y32T09P1	Transistor sink, 12 to 24V DC, 32 points, 0.12A/point, 3.2A/common	Connector	○
	NP1Y64T09P1	Transistor sink, 12 to 24V DC, 64 points, 0.12A/point, 3.2A/common	Connector	○
	NP1Y08U0902	Transistor source, 12 to 24V DC, 8 points, 2.4A/point, 4A/common	Screw terminal	○
	NP1Y16U09P6	Transistor source, 12 to 24V DC, 16 points, 0.6A/point, 4A/common	Screw terminal	○
	NP1Y32U09P1	Transistor source, DC12 to 24V, 32 points, 0.12A/point, 3.2A/common	Connector	○
	NP1Y64U09P1	Transistor source, 12 to 24V DC, 64 points, 0.12A/point, 3.2A/common	Connector	○
	NP1Y08S	SSR, 100 to 240V AC, 8 points: all points independent, 2.2A/point, 2.2A/common	Screw terminal	—
	NP1Y06S	SSR, 100 to 240V AC, 6 points, 2.2A/point, 4.4A/common	Screw terminal	○
	NP1Y08R-04	Relay, 110V DC, 240V AC, 8 points, 30V DC/264V AC: 2.2A/points, 4A/common	Screw terminal	○
	NP1Y16R-08	Relay, 110V DC, 240V AC, 16 points, 30V DC/264V AC: 2.2A/point, 8A/common	Screw terminal	—
	NP1Y32T09P1-A	Transistor sink, 12 to 24V DC, 32 points, 0.12 A/point, 3.2A/common, pulse output	Connector	○
Digital input/output module	NP1W1606T	24V DC 8 points, source input, 12 to 24V DC 8 points transistor sink output	Screw terminal	○
	NP1W1606U	24V DC 8 points, sink input, 12 to 24V DC, 8 points transistor source output	Screw terminal	○
	NP1W3206T	24V DC 16 points, source input, 12 to 24V DC, 16 points, transistor sink output	Connector	○
	NP1W3206U	24V DC 16 points, sink input, 12 to 24 V DC, 16 points, transistor source output	Connector	○
Analog input module	NP1AXH4-MR	High-speed multi-range input 4 channels, resolution: 14-bit	Screw terminal	○
	NP1AX04-MR	Standard multi-range input, 4 channels, resolution: 10-bit	Screw terminal	○
Analog output module	NP1AYH2-MR	High-speed multi-range output, 2 channels, resolution: 14-bit	Screw terminal	○
	NP1AY02-MR	Standard multi-range output, 2 channels, resolution: 10-bit	Screw terminal	○
Power supply module	NP1S-22	100/240V AC input power source, 35W, 2 slot size	——	○
	NP1S-42	24V DC input power source, 35W, 2 slot size	——	○
Baseboard	NP1BP-13	No. of slots=13, No. of processor bus slots=10	——	○
	NP1BS-06	No of slots=6, No. of processor bus slots=3	——	○
	NP1BS-08	No. of slots=8, No. of processor bus slots=3	——	○
	NP1BS-11	No. of slots=11, No. of processor bus slots=3	——	○
	NP1BS-13	No. of slots=13, No. of processor bus slots=3	——	○

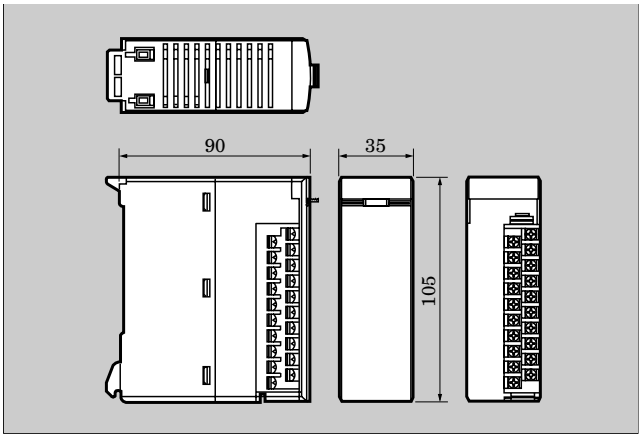
(4) Monitoring functions of the SX bus

The reliability of serial transmission is improved by such RAS functions in a custom LSI as CRC error checking, undefined frame monitoring, frame length monitoring and symbol fault monitoring on the lines, as well as over-run and under-run detection in the line interfaces.

4.2 The processor bus

The processor bus is a dedicated data bus that provides high-speed direct access to the global variables between the CPU modules as well the global variables between the CPU modules and the P/PE link modules. Connection of a maximum of 10 stations is

Fig.4 Appearance of input/output module



possible.

High-speed data transfer between the multi-CPUs is made possible by placing the processor in parallel with the I/O transfer of the SX bus.

5. Input and Output Modules, Power Supply Modules and Baseboards

As shown in Table 3, several types of input and output modules, power supply modules and baseboards have been newly developed to realize high-performance of the SPH.

5.1 The input and output modules

For process input and output (I/O), several modules for digital input and output (DI/DO) as well as analog input and output (AI/AO) are provided.

The main technical subjects encountered in the development of I/O modules are downsizing and countermeasures against heat generation and electrical noise (EMC).

To solve these subjects, a multi-layered printed circuit board (4 layers) and hybrid components were utilized.

Moreover, the number and arrangement of components as well as the wiring pattern was optimized based on the results of thermal analysis, EMI simulation and noise emission analysis.

These measures have achieved downsizing of 65% in volume compared with the conventional models (MICREX-F70), satisfactory input and output performance and good EMC characteristics.

Figure 4 shows the external view of the input and output module.

5.2 The power supply module

The dedicated power supply module for the SPH features small-size, high-power and parallel operation.

Since the SPH provides a single 24V power supply to each module via the baseboard, the necessary power supply capacity can be calculated simply by summing the currents consumed for each module.

Table 4 General specifications of the scalable multi-controller SPH

Parameter		Outline of specification
Physical environmental conditions	Operating ambient temperature	0 to 55 °C
	Storage temperature	– 25 to +70 °C
	Relative humidity	20 to 95% RH, no condensing
	Pollution degree	Pollution degree: 2
	Anti-corrosiveness	No corrosive gas No organic solution
	Operating altitude	Below the altitude 2,000m
Mechanical service conditions	Vibration	Vibration width : 0.15mm Constant acceleration : 19.6 m/s^2
	Shock	Peak acceleration: 147m/s^2
Electrical service conditions	Noise immunity	Square wave : 1.5kV
	Electrostatic discharge	Contact : 6kV Atmosphere : 8kV
	Radio-electrostatic immunity	10V/m
Construction		Rack-mounted type
Cooling		Air cooling
Dielectric property		Described for each module

One module supplies sufficient power for normal use. Even if modules that consume large amounts of power are combined, since the power source capacity is easily increased by parallel operation, it is not necessary to provide various power sources with different capacities.

Parallel operation is useful to not only increase the power source capacity but also for redundancy of the power supply. For example, if two power sources are used redundantly, the controller can continue operation, even if one of them breaks down.

5.3 The baseboard

The baseboard has a simple construction using extruded aluminum. Its size ranges from 6 to 13 slots.

One pair of SX bus expansion connectors attached to the left end of the baseboard makes it possible to structure a large-scale controller system by connecting multiple baseboards.

The baseboards are connected to each other with the SX bus extension cable that can be extended to a maximum length of 25m. Combining the T-branch unit with various types of baseboards results in improved flexibility for placement of the controllers.

The SX bus and the processor bus connect to the slot of baseboard. The NP1BP-13 model, with 10 slots for processor buses, is provided to configure high-speed multi-CPU systems with many CPUs. If multiple baseboards are provided, one or more power sources

are connected to each baseboard.

6. Design and Structure

The SPH has an easy to use, compact structure with an elegantly rounded front face. It is not only compact, but also easy to assemble and does not require screws. The materials used are friendly to the environment.

6.1 Design concept

Design concepts for the scalable multi-controller SPH included: small size and compactness, scalability, sturdiness, versatile functions, safety, harmony with the environment, and differentiation.

The design concept that integrates the above items is scalable and solid, giving an impressive sense of unification and high integration.

6.2 Assembly without screws

A structure without screws, such as the MICREX-F70, fixes the SPH module to the baseboard.

Through the use of extruded aluminum materials and development of a new method of attaching the modules, high vibration resistance and an easy-to-attach construction was realized.

6.3 Attaching with the DIN rail

The baseboard can be attached to the control panel either by screws or by DIN rails.

To attach the baseboard to the control panel by a DIN rail, the baseboard hooks onto the rails, and then both ends are fastened by metal fittings.

If attaching by screws, use of the metal fastenings simplifies the fixing work.

6.4 The terminal block using M3 screws

M3 screws are used at terminal blocks (I/Os) to achieve downsizing and simplify the wiring work. A maximum of 20 poles can be equipped on a screw type terminal block.

The wiring for modules having 32 or more input and output points is done with connectors.

7. General Specifications

The specifications of the scalable multi-controller SPH are adequate to fully withstand various severe industrial environments. (See Table 4.)

Moreover, the hardware and software conforms to IEC 61131 (JIS B 3500-3), the international standard for PLCs. Qualification has been applied for in the following standards:

(1) CE markings
(2) UL, cUL
(3) NK, Lloyd

In recent years, EMC has been strictly regulated. However, as the result of repeated EMI simulations, measurements and countermeasures, the MICREX-SX product series meets those standard values.

8. Conclusion

The specifications and features of the scalable multi-controller SPH (hardware PLC), the core of the MICREX-SX series, has been introduced.

Future development will strive to expand the product line, and improve functionality and performance of the MICREX-SX series.