Second-Generation PDP Address Driver IC

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1. Introduction

Color PDPs (plasma display panels) are used in household TV sets because of their distinctive features of thin profile, light weight and wide viewing angle. However, cost reduction of color PDP is an essential pre-condition for it to achieve higher market penetration. Recently, BS (broadcasting satellite) digital broadcasts were launched, and the market is expected to demand higher definition PDPs suitable for digital high vision.

To realize high performance and low cost PDPs, it is essential to improve the driver IC (integrated circuit) technology, in addition to improving the panel technology. Demands have increased for driver ICs having lower cost together with higher performance, such as higher speed switching, lower power consumption, and higher noise resistance.

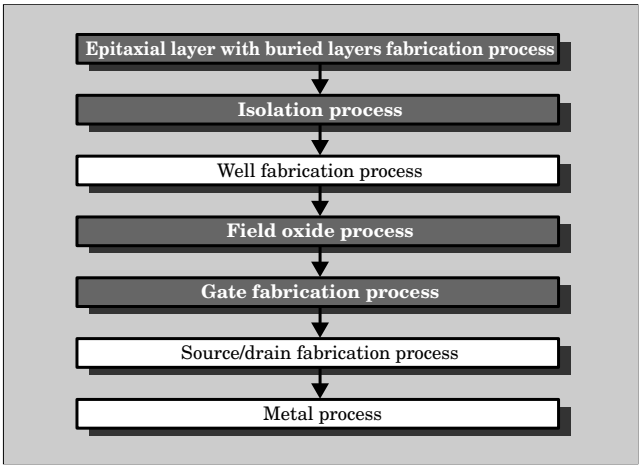
Fuji Electric has been manufacturing scan driver ICs[(1)] that utilize a dielectric isolation process and address driver ICs[(2)] that utilize a pn junction isolation process as the first-generation PDP driver ICs. Now, we are undertaking the development of second-generation PDP drivers, having even higher performance and lower cost, to realize high performance and low cost PDPs. We recently developed a second-generation PDP address driver IC having a 70 V operating voltage.

This paper introduces a brief overview of the device / process technology and the characteristics of the second-generation address driver IC.

2. Process Technology

During development of the second-generation PDP address driver ICs, we made an effort to decrease on-resistance and reduce the isolation area to realize lower cost. Figure 1 shows an outline of the process flow. The flow is based on a 1 μm-rule logic CMOS process and the shaded parts of the process were improved from the existing method. We optimized the pn junction isolation process that utilizes an epitaxial wafer with buried layers, which has been adopted from the prior product. We also improved the field oxidization and gate fabrication processes based on the existing process. Die size was miniaturized by the introduction of a double metal process. (Prior products utilized a single metal process.) As a result, the targeted performance and miniaturization of the die were both realized.

Fig.1 Overview of the process flow



3. Device Technology

As high-voltage devices, we developed lateral type n-channel MOSFETs (metal oxide semiconductor field effect transistors) (NMOS) and p-channel MOSFETs (PMOS) that guaranteed a switching voltage of 70 V. As a result for both IC devices, we achieved higher current capacity per unit element area and reduced the die area. Also, as the control circuit device, we developed a CMOS (complementary MOS) device having a switching capability of 40 MHz. This device has a breakdown voltage of more than 12 V between drain and source terminals. The following is a brief description of the high voltage devices.

3.1 High voltage devices

3.1.1 Current-voltage characteristics

In a PDP driver IC, the output circuit consisting of high voltage device occupies more than 50 % of the die area. Therefore, the die area occupied by the high

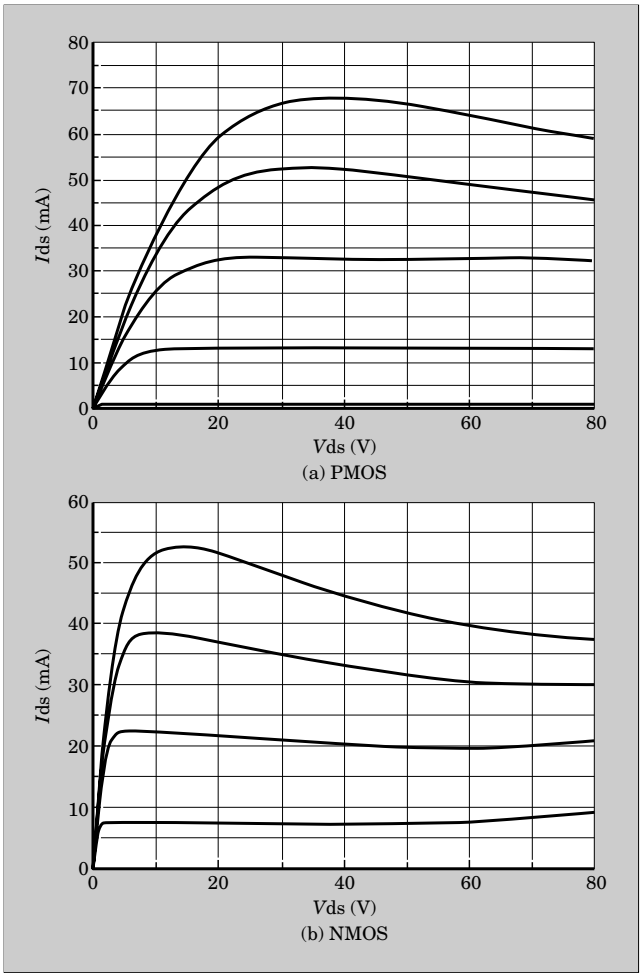
voltage device must be reduced to achieve miniaturization of the PDP driver IC.

Figure 2 shows the current-voltage characteristics of NMOS and PMOS devices developed by Fuji Electric. Current driving capacity per unit element area was increased as the result of reducing the active area by lowering the on-resistance of the element and by miniaturizing the isolation area through improved fabrication techniques. For the purpose of lower on-resistance, we incorporated the following improvements without introducing a complex element structure.

(1) Improvement of trade-off characteristics between breakdown voltage and current driving capacity by modifying the drain layer fabrication method
(2) Reduction of channel resistance by modifying the method of channel region fabrication
(3) Miniaturization of cell size by modifying the element cell pattern and optimizing the device parameters

For the NMOS device, we increased the impurity density of the drain layer by means of the resurf effect[3].

Fig.2 Current-voltage characteristics of high-voltage devices



3.1.2 Reliability characteristics

To verify the quality of the devices, we performed a high temperature reverse-bias reliability test (HTRB test) on each device element. The applied voltage was 70 V and the tested temperature was 150°C. Figure 3 shows the current characteristics of the NMOS and PMOS devices during the HTRB test. For both devices, the initial current remained unchanged after testing for 2,000 hours. The breakdown voltage of both devices also remained unchanged though it is not shown in Fig. 3. Since device characteristics were unchanged after the HTRB test, we were able to verify the quality of the devices.

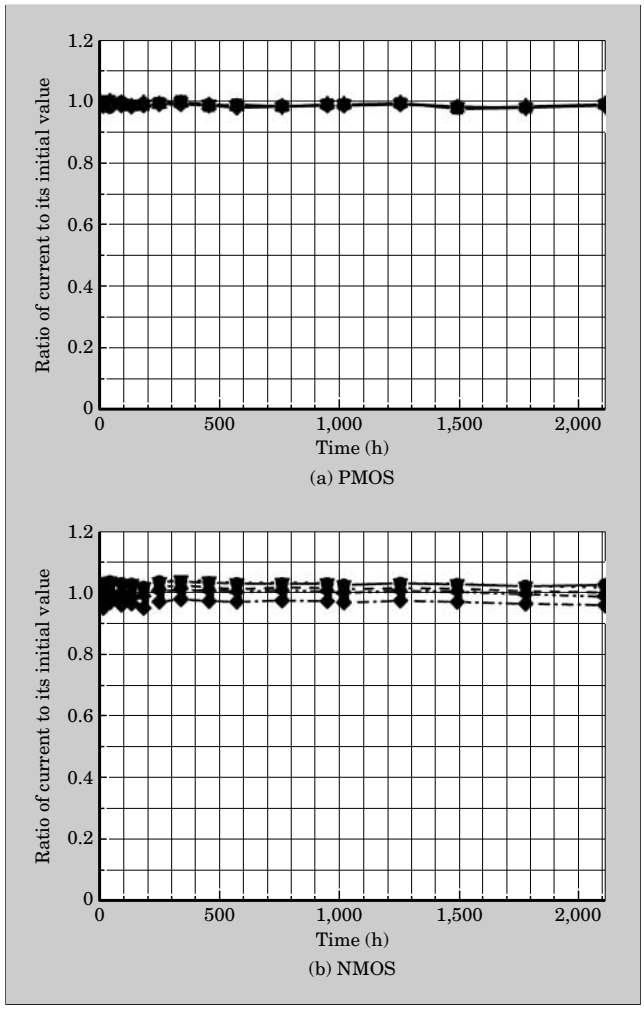
4. Application of Color PDP Driver IC

We also developed a color PDP address driver IC, using the distinctive processes and devices we developed.

4.1 Overview

Principal characteristics of this IC device are as follows:

Fig.3 Current characteristics of high voltage devices under the HTRB test



(1) 128-bit high voltage push-pull output
(2) High voltage output: 85 V (maximum), ±30 mA (typical)
(3) High voltage high speed switching
(4) High speed data transfer:
40 MHz (Maximum for data latching)
26 MHz (Maximum for a cascade connection)
(5) 3.3 V CMOS input interface
(6) 4-bit data input / output ports
(7) Four 32-bit bi-directional shift register circuits

4.2 Block diagram

Figure 4 shows a block diagram of the developed IC.

The circuit is comprised of an input buffer circuit for the interface with 3.3 V CMOS input, four bi-directional 32-bit shift register circuits, a 128-bit latch circuit, a gate circuit for controlling all high voltage outputs H/L/Z (high/low/high impedance), a low static current dissipation level shift circuit and a 128-bit high voltage push/pull output circuit.

4.3 Features and comparison with the prior product

4.3.1 Die size

Figure 5 shows a photograph of the developed IC.

Die area per output circuit of the IC was reduced to 61 % of the prior product through the adoption of newly developed low on-resistance devices and minute precise processing methods, and by increasing the number of high voltage outputs (128 outputs compared to 64 outputs for the prior product).

Fig.4 Block diagram

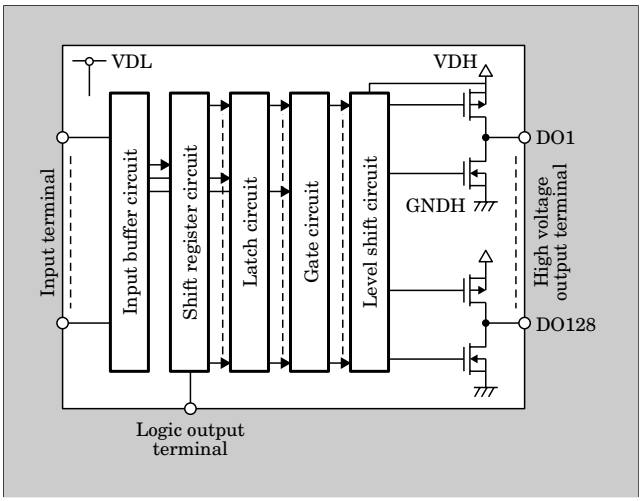
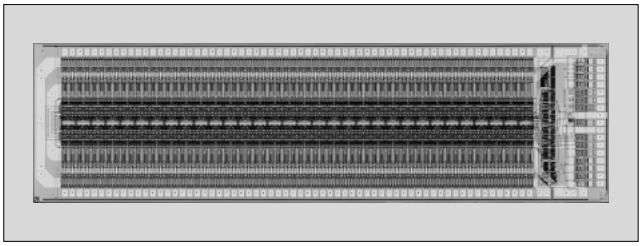


Fig.5 Photograph of a developed IC



4.3.2 Main characteristics

Table 1 shows the main characteristics of the developed IC and prior product.

(1) High and low level output voltage

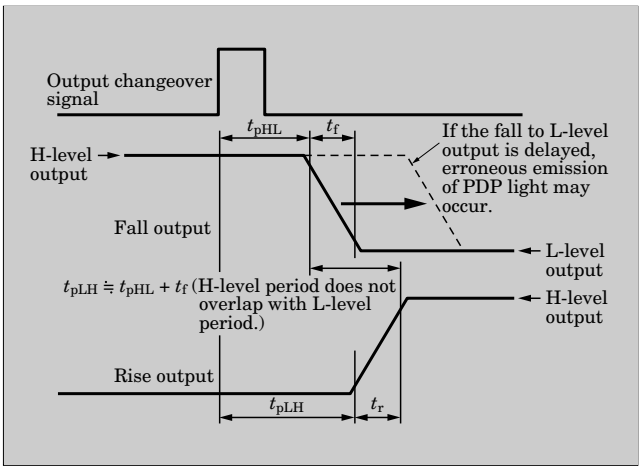
The high-level output voltage circuit has characteristics equivalent to those of the prior product. The on-resistance of the low-level output voltage circuit has been reduced by half. This characteristic relates to the heat dissipation and affects the die size greatly. Thus, the miniaturization and improvement of the IC charac-

Table 1 Comparison of main characteristics

Description	Symbol	Condition /application	Prior product	New product	Unit
High level output voltage	$V_{OH\,DO}$	I OH = –30 mA (High voltage output)	64.0	64.8	V
Low level output voltage	$V_{OL\,DO}$	I OH = 30 mA (High voltage output)	5.0	2.2	V
Static current dissipation	I_{CC}	Logic source current	6.6 (mA)	1.0	μA
	I_{DD}	High voltage source current	6.6 (mA)	1.0	μA
Maximum clock frequency	f_{CLK}	Data latch	40.0	50.0 or more	MHz
		Cascade connection	40.0	50.0 or more	MHz
Transmission delay time	t_{pdHL}	Logic output	19.0	14.2	ns
	t_{pdLH}	Logic output	22.4	15.3	ns
	t_{pHL}	High voltage output	91.8	55.8	ns
	t_{pLH}	High voltage output	156.0	130.0	ns
Output rise time	t_r	High voltage output	146.0	52.3	ns
Output fall time	t_f	High voltage output	113.0	75.6	ns

Note: Unless otherwise specified, T_j =25°C, V_{DL} =5 V, V_{DH} =70 V

Fig.6 High voltage output characteristics



teristics were realized.

(2) Static current dissipation

By improving the level shift circuit, the static current dissipation of 6.6 mA for the prior product was reduced to less than 5 μA.

(3) Switching speed

High-speed switching is essential for realizing high-definition PDP. We succeeded in speeding up the logic circuit by employing minute precision processing and achieving a high voltage output by improving the level shift circuit.

Other distinctive features of the new IC are that, even in the high speed switching circuits, the rising period does not overlap with falling period during the transition from a high-level period to a low-level period and vice versa ($t_{pLH} \fallingdotseq t_{pHL} + t_f$), and the undesired emission of PDP light is prevented as shown in Fig. 6. This feature was realized through control of the transmission delay time. In the PDP, light is emitted only for those bits which are output from the data driver at a high-level. Therefore, it is desired that bits to be turned off drop down very quickly to low-level output.

5. Conclusion

In this paper, we introduced the major features and process/device technology of the second-generation PDP address driver IC developed by Fuji Electric, and which are based on the pn junction isolation process.

For the application of PDPs to household TV sets to become widespread, higher performance and lower cost are essential. New driver IC technology for the PDP has to be developed for this purpose. Fuji Electric will continue to develop high performance and low cost driver ICs with distinctive features in accordance with market needs.

References

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