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UNIVERSAL SEQUENCE CONTROLLER (USC-4000)

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I. INTRODUCTION

Sequential control is the most popular technique used in automation, and the range of applications and demand for such equipment is steadily increasing with the increase in automation and increased sophistication and diversity of the control objectives evident in recent years.

On the other hand, a sequence (schematic) and construction drawing (parts layout diagram) and wiring diagram (wiring table) are prepared together with arrangement of the required parts, and the sequence controller is designed and produced by installing and wiring the parts in accordance with these diagrams. However, since these steps cannot be omitted in each equipment and one set of operations are performed almost in series, design and production require a large amount of time and labor. Moreover, since the control contents are determined by the actual circuit construction of the equipment in this method, modification and expansion of the control objective is impossible and it is thus inflexible. Therefore, both manufacturers and users desire the development of a general purpose sequence controller which can use the same standardized hardware without regard to the control contents. We are already manufacturing the "Universal Sequence Controller USC–500" stored program general purpose sequence controller to meet this need. Since the logical construction of the sequence controller is determined by the program memory pattern in the stored program system, the hardware can be standardized.

The USC–4000 is a stored program general purpose sequence controller the same as the USC–500, but incorporates such improvements as the extensive use of IC, the addition of a timer function and internal memory, simplified programming, and other function improvements which make it suitable for use in general sequential control.

II. FEATURES

The development of the USC–4000 was based on our wide experience in sequential control and computer control of powers and industrial facilities and has the following features.

1. Circuit Elements

TTL, HTL, and discrete transistors have been used to reduce size and increase reliability, and the noise margin has been increased through the use of HTL and transistors in the high noise level I/O circuit.

2. Circuit Construction and Reliability

Erroneous operation is prevented and mulfunctions are automatically detected by duplication of the main circuit and a self diagnosing circuit. The equipment is halted in the preceding state and a lamp which permits determination of the trouble point is lighted when a mulfunction occurs.

3. Input Circuit

The input circuit employs a unique pulse transformer system, and circuit construction is not only simple, but also reliable and is isolated from the external circuits with respect to DC. Moreover, the input circuit can use DC 110 V. The effects of noise and faulty input signal contact can be prevented by using DC 110 V. Moreover, DC 24 V is utilized in contactless relay, and other connections (Patent pending).

4. Operation Function

The logical operation and timer functions indispensable in sequential control are provided, and it is thus applicable to general sequential control applications. Up to a maximum of 128 timers can be equipped by means of a unique system and time setting can be performed by program. (Patent pending)

5. Programming

Since there are only four types of instruction words directed toward sequential control and the instruction system has been simplified, is extremely easy (Patent pending).

Moreover, since the program memory is a core memory, writing-in and modifying the program are easy.

6. System Construction

Since it is designed exclusively for use as a sequence controller, there is little redundancy compared with cases in which a minicomputer are applied to sequential control. Moreover, since the I/O interface has also been designed for sequential control, system construction is simple and low cost.

This system has a maximum of 255 I/O channels. This scale is based on the fact that from our experience up to now, a large part of sequential control is on this scale and on the concept that control should be divided into a number of groups from the stand point of reliability in large scale systems. Moreover, the number of I/O channels, number of timers, and number of program steps can be selected in a building block system corresponding to the system scale.

7. Wide Flexibility and Applicability

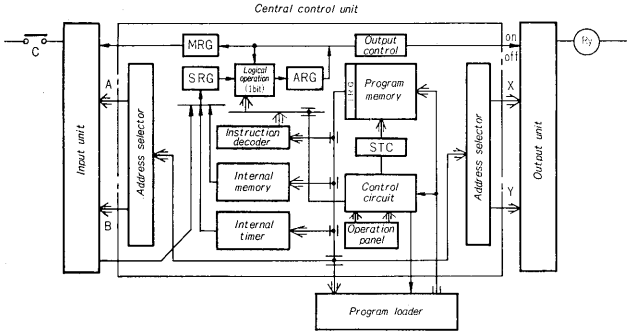
Since the control contents can be set by means of only the program, control modification with respect to alteration and expansion of the control objective are easy and highly flexible. Moreover, a higher function control system can be constructed by combining with analog control equipment, numerical control equipment, and other control equipment and can take charge of sequential control as a system component of a computer control system.

8. Handling Ease

Programming and handling are extremely easy, and can be easily used by those in charge of sequential control of electromagnetic relays, solid state switching relays without any special knowledge required.

III. EQUIPMENT CONSTRUCTION

The equipment comprises a central control unit, I/O unit, power supply unit and program loader as shown in *Fig. 1*. The central control unit has the functions of common operation, the I/O unit is the interface between the equipment being con- trolled and the control unit, and the program loader writes in the program and prints out the contents of the program.



MRG: Operation memory (1 bit) ARG: Accumulator
IRG: Instruction registor SRG: Signal registor
STC: Step counter

Fig. 1 System structure of USC-4000

1. Equipment Specifications

The specifications of each unit and the instruction words for programming are given in *Table 1* and *Table 2*.

Table 1 **Specifications of the USC-4000**

Control system	Synchronous control	
Program system	Stored program	Program setting by key or program loader
Instruction system	1 address system	
Number of instruction	4 (basic)	See Table 2
Word length	12 bits+parity bit	Total 13 bits
Operation system	Cyclic operation	
Operating function	Logical operation timer	
Program step	2048 or 4096	
Operation time	8μ sec/1 instruction	
Memory	128 bits (1 bit memory)	With central control unit
Timer	Max. 128 points 0.1~25.5 sec., 1~255 sec.	With central control unit. Increase or decrease possible in 32 point unit
ON/OFF input	Max. 255 points Insulation test AC 2,000 V 1 min	Increase and decrease possible in 8 point unit Input current approx. 5 mA
ON/OFF output	Max. 255 points Solid state switch	Increase and decrease possible in 8 point unit Output capacity DC 24 V, 0.1 A
Power supply	AC 100-110, 200-220 V 50, 60 Hz	
Ambient condition	0~40°C 10~85% RH	
Accessory	Program loader	With symbolic keys and printer

Table 2 **Composition of the instructions**

Instruction		Symbol	Machine language	Instruction modification	Content of operation
Operation	READ	R	K 0 1 M N	M=0	(ARG)→MRG, (N)→ARG
				1	(ARG)→MRG, $(\overline{N})$→ARG
	AND	A	K 1 0 M N	0	(N)∧(ARG)→ARG
				1	$(\overline{N})$∧(ARG)→ARG
	OR	O	K 1 1 M N	0	(N)∨(ARG)→ARG
				1	$(\overline{N})$∨(ARG)→ARG
Control	WRITE	W	K 0 0 M N	0	(ARG)→N(±0), Not effective at N=0
				1	$(\overline{ARG})$→N(±0), End at N=0 *1

K: Parity bit I: Instruction
M: Instruction modification N: Address

Note: [ ] indicates contents of register, I/O, etc.
— indicates its negation
*1 indicates end of program, STC is set to zero
MRG can read at input address zero

2. Principles and Operation of the Equipment

A theoretical diagram of the equipment is shown in *Fig. 2.*

A sequence controller comprising magnetic relays, solid state switching relays, etc. connects the individual logic elements, memory (flip-flop, etc.) and timers by direct wiring in accordance with the specifications. On the other hand, in this equipment, the control informations are transferred at a time at high speed by means of an electronic switch from the input circuit, memory, timer to the common operation circuit and are logically operated in accordance with the program set in advance and based on the control specifications and then sent to the output points through a hold circuit. Since these operations are performed at extremely high speed, functions equivalent to those of the previously described relay type sequential control can be realized.

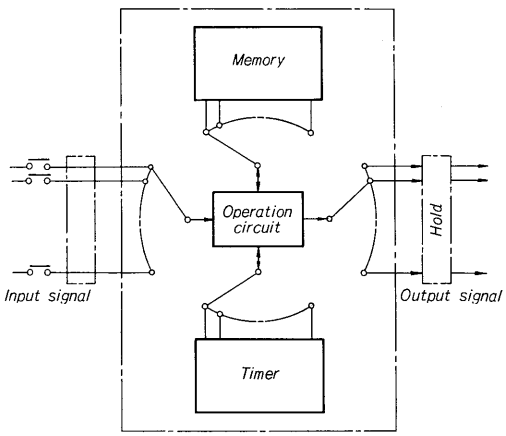


Fig. 2 **Basic operation diagram of USC-4000**

3. Central Control Unit

The central cotrol unit houses each of the function circcits described below. An external view is shown in *Fig. 3.*

1) Program memory

A nonvolatile read only memory (ROM) which permits easy electrical rewriting is ideal as the program memory element of this equipment. A so-called READ WRITE core memory having an ample record of use in computers, etc. and which also guarantees reliability is used in this equipment. Memory capacities of 2K and 4K are available. In order to improve reliability, an odd parity check is perform after the instruction is read from the program memory. Of course protection circuit which protects the memory when the power fails is also provided.

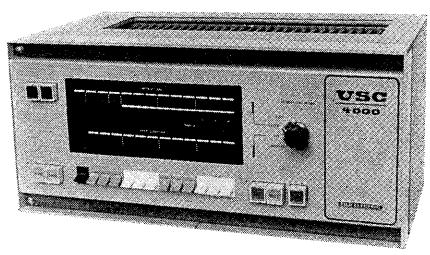


Fig. 3 **Central control unit**

2) Operation circuit

Considering a magnetic relay circuit as an example, all logical operation circuits can be constructed by combining the " a " contacts and " b " contacts in series or parallel. In this equipment, only AND and OR are used as basic operations and the instruction system has been simplified and the hardware reduced by performing all logical operations by adding a function which performs operations by inverting the input signal. A block diagram of the operation circuit is given in *Fig. 4.* In actual practice, there are two such circuits to improve reliability and check of matching of the operation results of the two circuits is performed constantly.

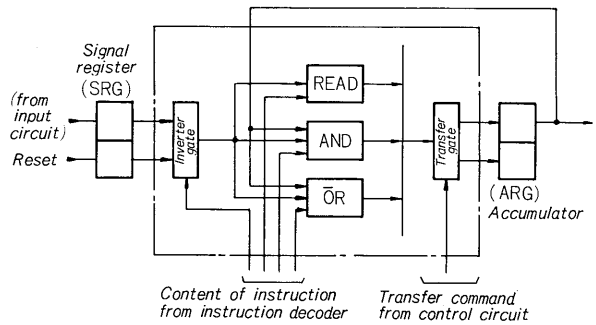


Fig. 4 **Logical operation circuit**

The following operations are performed in accordance with the decorded results of the instruction decoding circuit and the command from the control circuit :

READ : The contents of SRG are transferred to AGR (M=0)
The contents of SRG are inverted and transferred to ARG (M=1).

AND : The AND operation is performed on the contents of SRG and the contents of ARG and the result is transferred to ARG (M=0). The content of SRG are inverted, the AND operation is performed with the contents of ARG, and the result is transferred to ARG (M=1).

OR : The OR operation is performed on the contents of SRG and the contents of ARG and the result is transferred to ARG (M=0). The contents of SRG are inverted, the OR operation is performed with the contents of ARG and the result is transferred to ARG.

3) Input selecting circuit

A block diagram of the input selecting circuit is shown in *Fig. 5.* The input address is specified by bits No. 5～12 of the address part of the instruction

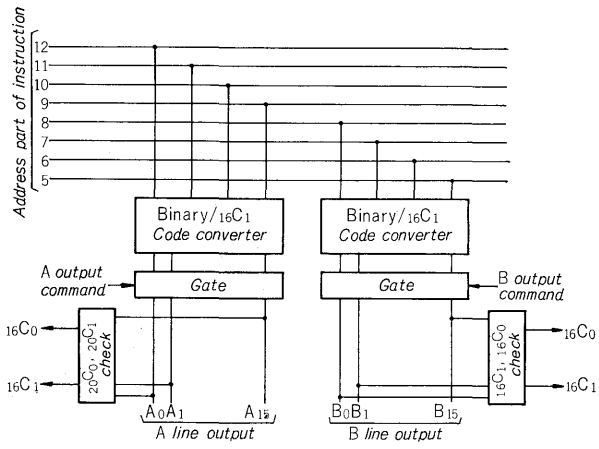


Fig. 5 Input selection circuit

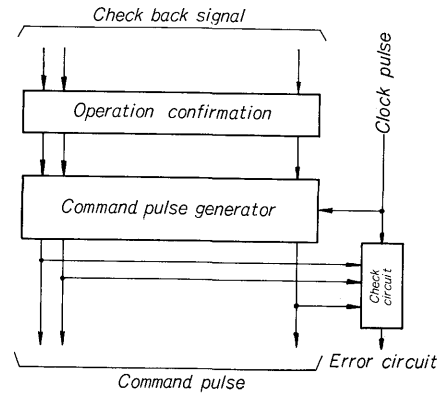


Fig. 6 Control circuit

register. In other words, $2^8=256$ points can be selected. This is divided into two groups comprising bits No. 5～8 and No. 9～12, and each binary code is converted to ${}_{16}C_1$ and connected to the input unit as an A line (A_0～A_{15}), B row (B_0～B_{15}) matrix signal. The output of the gate circuit is connected to ${}_{16}C_1$, ${}_{16}C_0$ detection circuits for checking. ${}_{16}C_1$ is a circuit which detects that only 1 of the 16 gates is ON, and ${}_{16}C_0$ is a circuit which detects that all 16 gates are OFF. The binary/${}_{16}C_1$ conversion circuit of this circuit is duplicated and an output signal is output only when the signals of both coincide. The output selecting circuit is identical to the input selecting circuit. The output address is specified by bits No. 5～12 of the instruction resister and connected to the output unit by converting bits No. 9～12 to an X line (X_0～X_{15}) and No. 5～8 to a Y row (Y_0～Y_{15}) matrix signal.

4) Internal memory circuit

This is 128 memories (each 1 bit) constructed from a semiconductor IC memory. The contents of ARG can be written into the memory specified by the address part by the WRITE instruction. In addition, direct operation between internal memory and ARG in the same manner as external input signals is possible and the inherent address is determined in the internal memory as described later.

5) Internal timer circuit

Up to a maximum of 128 timers using semiconductor IC memory can be equipped. The timer for 32 points can be mounted on 1 printed board, and the number can be increased and decreased in 32 point units.

Time setting can be performed by program. Range switching of 1 : 10 is possible by program, and time setting can freely specify the time within ranges of 0.1～25.5 seconds or 1～255 seconds in this way. Moreover, the inherent address is determined in the internal timer in the same manner as the internal memory.

6) Control circuit

This circuit gives control command pulses to each part of the equipment and confirms the operation of each part. Its block diagram is shown in *Fig. 6*. The basic operation of the control circuit consists of giving command pulses synchronized with the clock pulses to each part of the central control unit in accordance with the operating sequence, and employs a system which generates the next command pulse by confirming that correct response (operation confirmation, duplicated circuit check, parity check, etc.) has been received with respect to the command pulse. Therefore, when the above confirmation is not satisfied, the command pulse is not generated and the clock pulse and command pulse drop out of synchronized operation, this is detected by the check circuit, the equipment is stopped, and an alarm is given at the operating pannel. As described above, this equipment has a self diagnosing function and an abnormal condition can be easily known by means of lighting of the status indicator of the control circuit when the equipment is halted by a trouble. The one instruction processing time of this equipment is 8μs and maximum 4K step instruction processing time is approximately 32 ms and is sufficiently fast for practical use.

7) Output control circuit

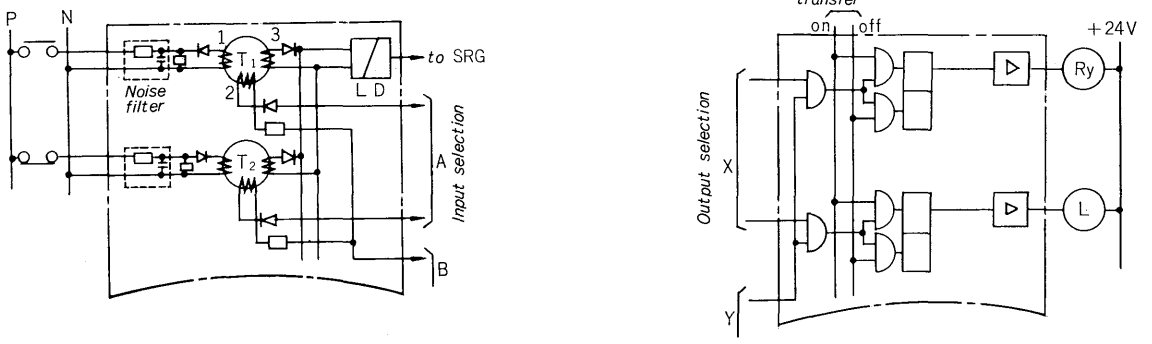
After the check circuit have confirmed that output selection has been performed correctly, the contents of ARG or it inverted contents (in the case of M= 1) are sent to the circuit which sends them to the output unit by means of the command pulse from control circuit to the output control circuit. The output unit only responds when both the address selection signal and output signal arrive simultaneously.

8) Operator's panel

The operator's panel is equipped with the operating switches required for normal operation or keys for loading of the program by machine language and lamps for checking the contents of the program.

4. I/O Unit

The I/O unit connects the central control unit with the equipment being controlled and consists of input and output printed boards and a frame which houses



(a) Input unit

(b) Output unit

Fig. 7 I/O unit

them. One set of frames can house 16 input and 16 output printed boards and 8 inputs or outputs can be connected per printed board. Since the I/O unit is the section directly connected with the equipment being controlled, ample studies have been conducted concerning noise immunity, insulation strength, etc.

1) Input circuit

As shown in *Fig. 7 (a)*, an impulse transformer is used and the circuit construction is extremely simple. Input circuit isolation is performed by means of winding 1 of the transformer, and selection reading of the input is performed by exciting winding 2 by means of the matrix signal (A line, B row) from the central control unit and detecting the voltage induced in winding 3 with a level detector LD.

Since a voltage is applied to the diode in the reverse direction when the input contacts are closed, the voltage pulse impressed on winding 2 is transferred to winding 3. Since the voltage induced in winding 1 from winding 2 is shorted by the diode and resistance when the input contact are open, there is almost no voltage induced in winding 3. Therefore, a "1" signal is sent to SRG of the central control unit only when an input signal (input contacts closed) is present.

The insulation test voltage of this circuit is AC 2000 V, 1 minute and a DC 100 V circuit can be directly connected. Current consumption is approximately 5m A.

Faulty contact of the external contacts is prevented and the noise margin (S/N ratio) is increased by making the input signal level DC 100 V, 5 mA and noise countermeasures are provided by installing a noise filter.

2) Output circuit

Circuit construction is shown in *Fig. 7 (b)*. The output is an open collector transistor switch and direct connection with the static switching circuit of another external system is possible. This circuit is generally connected to externaldevices through an auxiliary relay because of the relationship with the output capacity. The circuit is not a specially insulated type and is simple. An output capacity has been made DC 24 V, 0.1 A and is sufficient to operate an auxiliary relay directly. The output circuit only responds when the output selection signal (X line Y row) and output control signal are applied simultaneously.

3) Program loader

The program loader is used to write the program into the program memory of the central control unit. The program can be easily written and rewritten into the program memory by oprating symbolic keys.

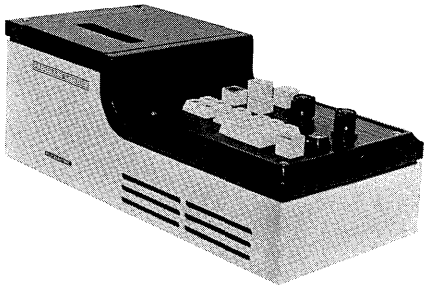


Fig. 8 Program loader

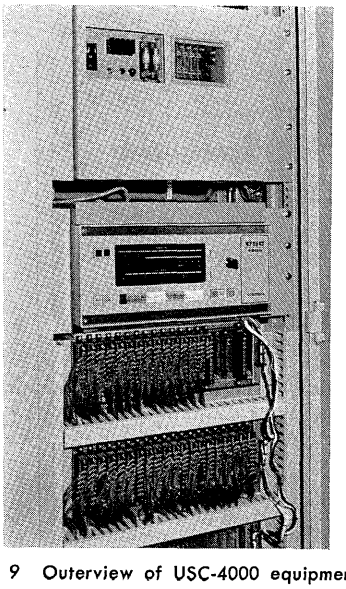


Fig. 9 Outerview of USC-4000 equipment

At this time, the content written into the program memory by key operation are automatically read out from the program memory and printed out by the internal printer, and then the contents of the program written in accordance with the key operation can be confirmed. In addition, since all the instructions in the program memory can be automatically printed out, program can be copied. An external view of the program loader is shown in *Fig. 8.*

4) Power supply unit

The power supply units supplies the power required by the central control unit and I/O unit and have a program memory protection function.

An outline of the construction of the USC-4000 has been given above. The external dimensions of each unit is given in *Fig. 9* and an external view of a usage example is given in *Fig. 10.*

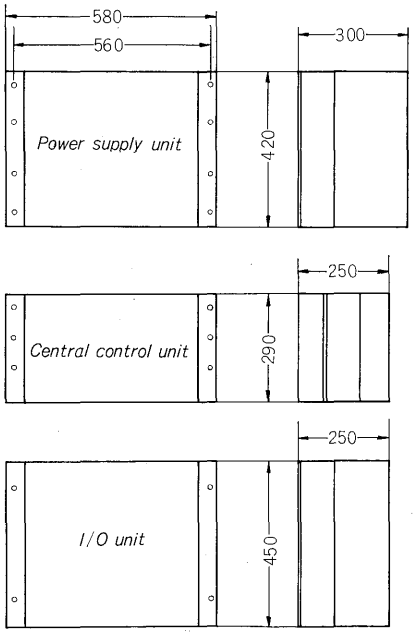


Fig. 10 Outerview of each unit

IV. PROGRAMMING

1. Instructions

The program for the objective control operation can be prepared by arranging instruction in the program memory in accordance with the control logic. The instructions are constructed by means of the 13 bit core memory as shown in *Fig. 11.* Parity check (odd check) is performed by bit 0 when reading the memory, bits 1～2 (abbreviated=I) are the operation code and bits 4～12 (abbreviated=N) specify the address.

Bit 3 is used to modify the instruction. The input signal logic is inverted and the operation specified by the operation code is performed when its contents are "1". The contents of the operation code are shown in *Table 3.*

The instruction part and address part of the instruction must always be specified and the address part is delimited in groups of 3 from bit 12 and read in octal. In the example in *Fig. 11*, I (0) 176 is shown and means the instruction which reads the input signal of address 176 into ARG as can be seen form *Table 3.*

Table 3 **Operation code**

Instruction	Symbol	Code	Function
READ	R	01	Load to ARG
AND	A	10	And
OR	O	11	Or
WRITE	W	00	Transfer from ARG

2. Setting of Timer

The desired time of the timer is set in the following step of the WRITE instruction for timer and is represented as shown in *Fig. 12.* In other words, the time is set by bit 8 of bits 5～12 and scaling set of the time is performed by the No. 3 bit. In the above example, (0) 225 is written and the set time in this case is 149 when octal 225 is converted to decimal, and since the scaler is 0.1, it becomes $149 \times 0.1 = 14.9$ (sec).

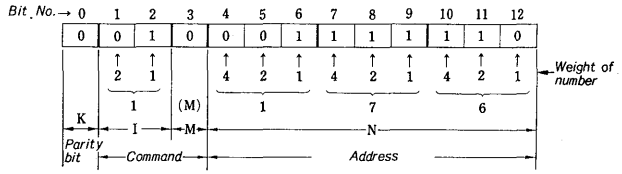


Fig. 11 Instruction code

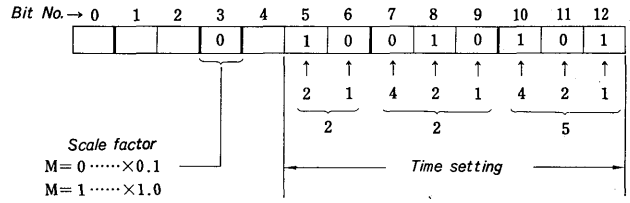


Fig. 12 Setting method of required time

Table 4 **Distribution of address**

Address (octal No.)	Use	
000	MRG (operation memory) address use as external I/O impossible	
001～377	I/O address	Imput address for READ, AND, OR instructions
		Output address for WRITE instruction
400～577	Internal memory address	
600～777	Internal timer address	

Time can be set up to 0.1～25.5 seconds in the case of scaler 0.1 (M＝0) and up to 1～25.5 seconds when scaler is 1.0.

3. Uses of the Address Sections

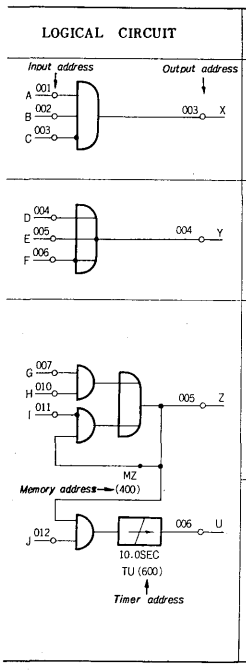
The inherent address sections usable as input, output, memory, or timer, are fixed as shown in *Table 4* in accordance with the hardware. We can use those individually by appointing the address in accordance with the program.

4. Program Representation Method

The program is finally arranged in the core memory as machine language, but in the program preparation stage, the symbols of the instructions of *Table 3* and the I/O signals are used. For example, representation as shown in *Fig. 13.*

When preparing the program, it is convenient to construct the logic circuits at first and whether this is done by writing with the logic circuit or by writing with the contact circuit can be determined at the side which prepares the program. In *Fig. 13*, the left item of the PROGRAM column is the symbol for the operation code and the right column is the symbol for the signal, and the symbol N represents negation. This corresponds to the instruction M＝1.

Moreover, the CODING column of the same figure is coding of SYMBOLIC PROGRAM and the program can be stored in the program memory by operating the program keys in I, M, N order.



LOGICAL EXPRESSION	STEP NO.	SYMBOLIC PROGRAM	I	M	N	
A・B・C̄=X	1	R－ A	R	0	001	
	2	A－ B	A	0	002	
	3	A－N, C	A	1	003	
	4	W－ X	W	0	003	
D+E+F̄=Y	5	R－ D	R	0	004	
	6	O－ E	O	0	005	
	7	O－N, F	O	1	006	
	10	W－N, Y	W	1	004	
(G・H)+(I・Z)=Z	11	R－ G	R	0	007	
	12	A－ H	A	0	010	
	13	R－N, I	R	1	011	(ARG)→(MRG)
	14	A－ MZ	A	0	400	
	15	O－ MRG	O	0	000	
	16	W－ MZ	W	0	400	
(Z・J)(TU)=U 10.0sec	17	W－ Z	W	0	005	
	20	A－ J	A		012	
	21	W－ TU	W		600	
	22	10.0		0	144	
	23	R－ TU	R		600	
	24	W－ U	W		006	

Fig. 13 Example of program

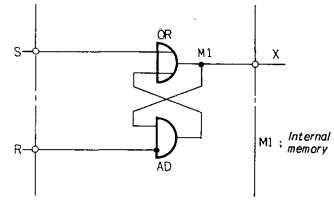
5. Programming Fundamentals

1) Program operation sequence

The program arranged in the program memory is sequentially executed from step 0. When the END instruction (I＝0, M＝1, N＝0 as shown in *Table 2*) arrives, it is returned to step 0 and repeatedly executed by repeating the instruction in step number sequence. The center of operation is ARG and the results of operation are always stored in ARG and the contents of ARG are output.

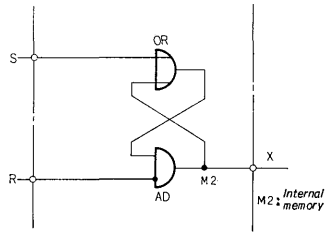
2) Initial setting of internal memory

When initially started by applying power to this equipment or when the reset pushbutton of the central control unit is pushed, the internal memory used by the program is rest to all "0".



STEP NO.	SYMBOLIC PROGRAM	
1	R－N,	R
2	A－	M1
3	O－	S
4	W－	M1
5	W－	X

(a) Set preferred Flip-Flop



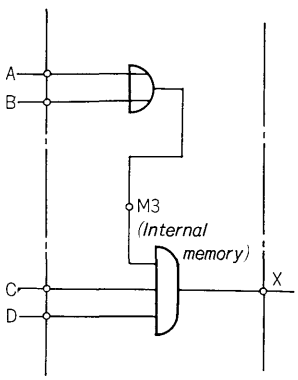
STEP NO.	SYMBOLIC PROGRAM	
1	R－	S
2	O－	M2
3	A－N,	R
4	W－	M2
5	W－	X

(b) Reset preferred Flip-Flop

Fig. 14 Applications of internal memory (part 1)

3) Internal memory

There are two usage methods. The No. 1 usage method is used when producing self holding circuits and flip-flop circuits and an example is shown in *Fig. 14.* Connecting the program as shown in *Fig. 15* can be used as the No. 2.



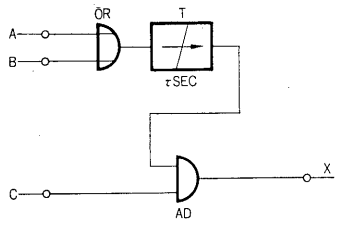
STEP NO.	SYMBOLIC PROGRAM	
1	R－	A
2	O－	B
3	W－	M3
	Other programs	
n	R－	M3
n+1	A－	C
n+2	A－	D
n+3	W－	X

Fig. 15 Application of intenal memory (part 2)

4) Internal timer usage methods

A typical timer program is shown in *Fig. 16.* Timer starting is performed by the WRITE instruction as shown at step 3 of the same figure. When the contents of ARG are "1" ("0" in the case of

M=" 1 "), the time given by the instruction after the WRITE instruction that is at step 4 and the timer output becomes 1 after the set time.



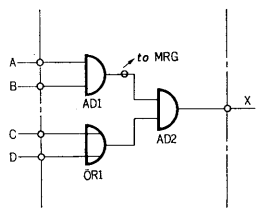
STEP NO.	SYMBOLIC PROGRAM
1	R− A
2	O− B
3	W− T
4	τ
5	R− T
6	A− C
7	W− X

Fig. 16 Application of time

Moreover, when ARG is " 0 " (" 1 " in the case of M=" 1 "), the WRITE instruction is executed, the the timer output becomes " 0 " and the timer is rest. Since the internal timer is theoretically a digital timer, when the scaler is 0.1, a error of +1.0 second is included. The timer output is initially reset under the same conditions as the internal memory.

5) MRG (operation memory)

MRG is one of the features of this equipment and permits a reduction in program steps. When the READ instruction is executed, the contents of ARG prior to execution are transferred to MRG and the new contents specified by the address part are read into the ARG. Since the output of MRG is connected to address 0 of the input, it can be used as follows.



STEP NO.	SYMBOLIC PROGRAM	
1	R− A	
2	A− B	
3	R− C	(ARG) →MRG
4	O− D	
5	A− MRG	
6	W− X	

Fig. 17 Application of MRG

In other words, since the AD1 operation is performed at steps 1 and 2 in *Fig. 17* and the result of AD1 is temporarily stored in MGR when input " C " is read into ARG at the next step 3, when the next AD2 operation is performed, in other words, at step 4, the operation of AD2 can be performed between MRG and ARG (output of OR1 entered).

6) No effective instruction and end instruction

If we let M=0, N=0 at the WRITE instruction as shown in *Table 2*, we get the no effective instruction and the central control unit does nothing. (" 1 " is entered in only bit 0 of the machine word and " 0 " is entered in all the other bits.) This instruction can be used when leaving blank program steps considering modification of the program or modification in the future.

The end instruction should be M=1, N=0 at the WRITE instruction and when the step of this instruction arrives, the step counter (STC) is reset to step 0 and the program is executed again from step 0.

7) Definition of ON, OFF signals

When the contacts of the input circuit are closed and the specified voltage is applied to the input point, the input signal is made " 1 ". The closed condition of the transistor switch of the output unit is defined the output signal as " 1 ".

The application of programmable general purpose sequence controller based on new design concepts widely incorporating recent electronic circuit techniques with respect to the conventional sequential control produced product by combining electromagnetic relays and solid state logical elements is flourishing with both manufacturers and users. This controller can be also widely used as a system component in large scale control systems including sequential control, analog control and computer control. Moreover, refer to the Fuji Electric Review Vol. 18 No. 1 Fuji programmable sequence controller " PROGIC " for application to comparative small scale sequential control.