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MOUNTING TECHNIQUE BASED ON BUMP TECHNOLOGY

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1. FOREWORD

Technological innovations in semiconductor manufacturing are made in the area of high integration of IC chips as represented by the memory IC. The innovation rate increases by nearly one and half to two times a year. In this way, making electrical devices smaller, lighter, and with higher density assemblies has been accelerated and spectacular progress has been made over the years. To realize the above mentioned developments, technological developments in such areas as high density assembly on the IC chip and the miniaturization, making light weight, and increasing the number of pins for the IC package have made a great contribution.

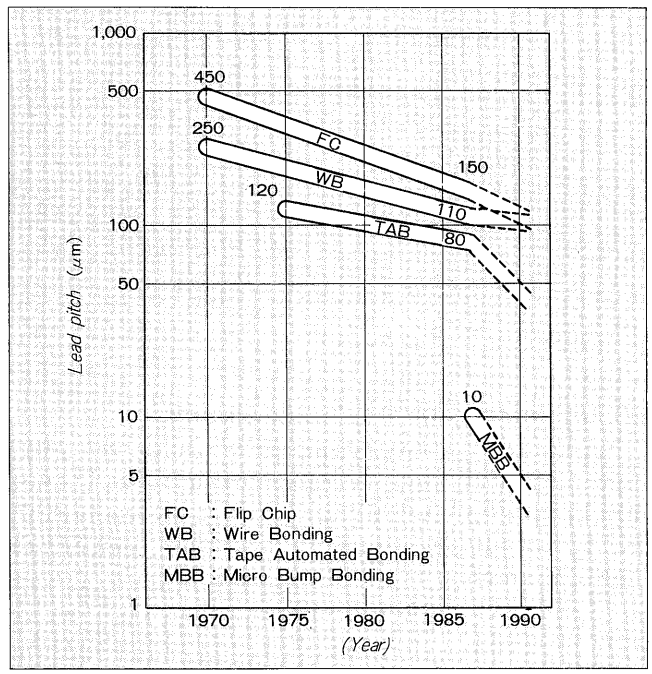
In recent years, in order to develop new equipment based on new needs and to improve the ability of currently produced equipment, ICs have come to be widely developed using new methods, to produce new high density assemblies which do not include packaging. Foremost among these new methods, the bumped chip method has been drawing the attention of the market since it does not require packaging but can be mounted on the surface of a circuit board and has the capacity for high density assembly.

At Fuji Electric, Ltd., development of flip chip (solder bump) was completed in 1979 and was put on the market as an ignition control IC for automobiles. From the beginning of its development, attention was focused on a high reliability design because it was to be used in a car. Specifically, we introduced a finite element method for the design of the bump. Furthermore, we developed an electrolysis plating method for high precision of the bump, and a high reliability passivation film formation method for the IC chip. Due to these developments, the bump is highly regarded even up to the present.

Pushing the technology further, a TAB (Tape Automated Bonding) gold bump was developed in 1980. With this development, we were able to enter into the information associated market. In this field also, the new bump technology has been highly valued.

As development continued, a DIP (Dual Inline Package) was completed in 1981 for the automobile ignition control IC so that the IC could withstand the harsh conditions it was subjected to. This technology was made into the standard for this field and the systematization of highly reliable packaging up to the 160-pin QFP (Quad Flat Package) was promoted and advanced. This paper presents products and packaging produced by Fuji Electric which involve this new bump technology.

Fig. 1 Lead pitch progress and estimated of IC chip assembly



2. BUMP TECHNOLOGY

In IC chip assembly, other than the usual method of wire bonding, there are the flip chip bonding method and the TAB method, both of which use the bump on chip technology. For electrical devices with greater ability, smaller in size, and lighter in weight, the flip chip and TAB methods have wide application. These assembly technologies each have advantages as concerns the specific application. Therefore it is necessary to separate them and to use the method which exhibits its special merit according

Fig. 2 Trend of high density assembly

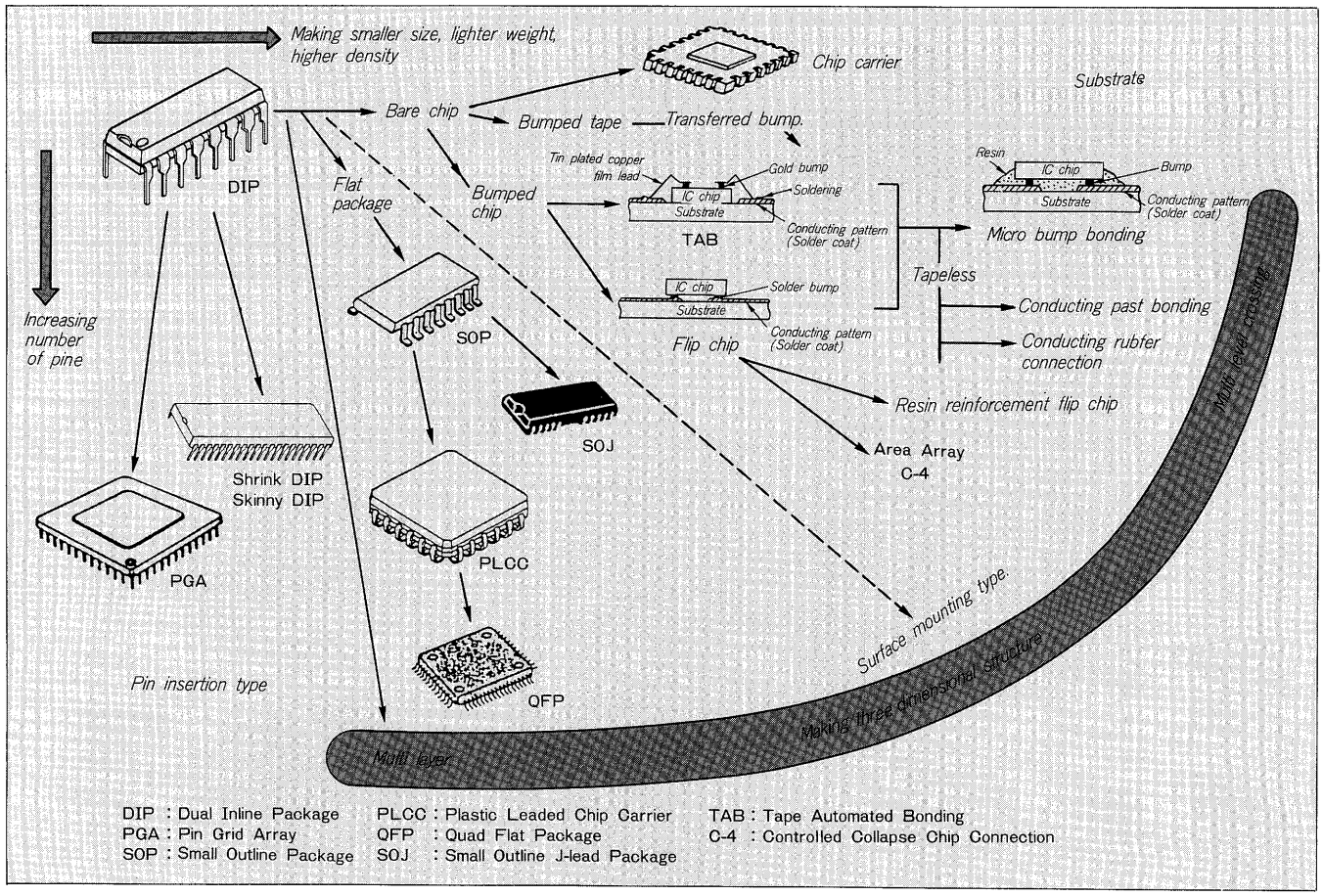
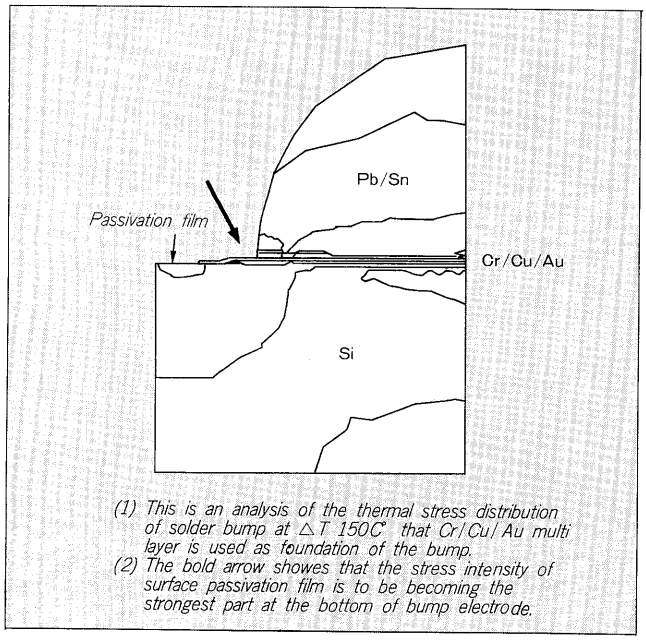
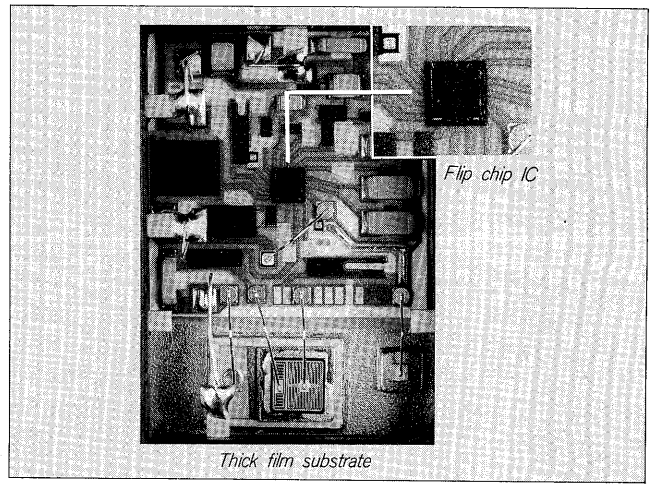


Fig. 3 A case of stress distribution analysis (Thermal stress distribution analysis of solder bump electrode by using the finite element method)



(1) This is an analysis of the thermal stress distribution of solder bump at △T 150C° that Cr/Cu/Au multi layer is used as foundation of the bump.
(2) The bold arrow showes that the stress intensity of surface passivation film is to be becoming the strongest part at the bottom of bump electrode.

Fig. 4 Hybrid IC used on automobile



to the product.

At Fuji Electric, Ltd., for applications requiring high reliability and high density assembly, flip chip ICs with solder bumps are used. Examples include hybrid ICs used on automobiles and driver ICs for displays. TAB ICs with gold bumps are used for thermal printers and also for panel display drivers. These products are being produced now and there are plans to expand these families to make them receptive to the new techniques.

Fig. 5 Driver IC for display

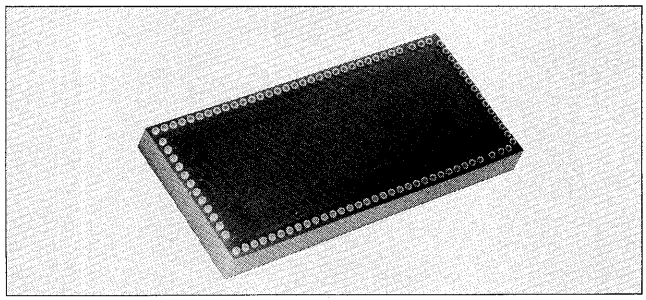
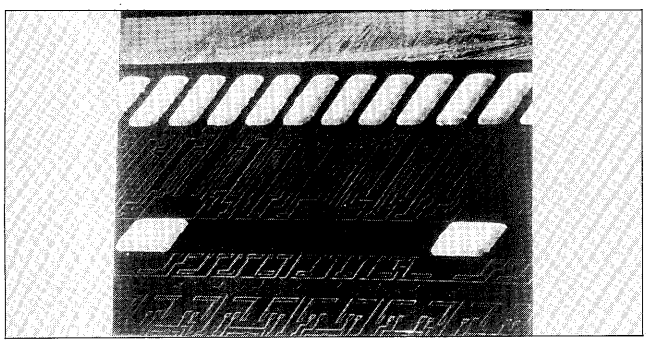


Fig. 6 Driver IC for thermal printer



2.1 Bump making process

The bump making process on the IC wafer is indicated in *Fig. 7*.

(1) Depositing Passivation Film on IC Wafer
(2) Making Through Hole on Passivation Film
(3) Depositing Bump Making Metals
(4) Patterning Electrolysis Plating Mask
(5) Bump Electrolysis Plating
(6) Selective Removal of Bump Metals Film

According to the process flow shown above, bumps are made on the IC wafer. As the IC is made more complicated with more functions, many bumps are needed on the IC wafer. Therefore, the size and pitch of the bumps are designed to the minimum limits.

2.2 Assembly method of IC chips

Assembly methods for IC chips are indicated in *Fig. 8*.

(1) Wire Bonding Method

IC chips are bonded with an adhesive agent to the substrate, and then each IC pad is wired with gold wire, etc., by a wire bonder.

(2) Flip Chip Method

IC chips are aligned on the substrate and are bonded with solder bump electrodes in a furnace. By this method many chips can be bonded at the same time.

(3) TAB Method

Copper leads plated with tin that are attached to heat-resisting tape are connected to the gold bump electrodes on the IC wafer (ILB: Inner Lead Bonding). Then the ILB area that is cut off from the tape is connected to the circuit substrate (OLB: Outer Lead Bonding). This method can do the middle step's test.

Fig. 7 Bump-forming process

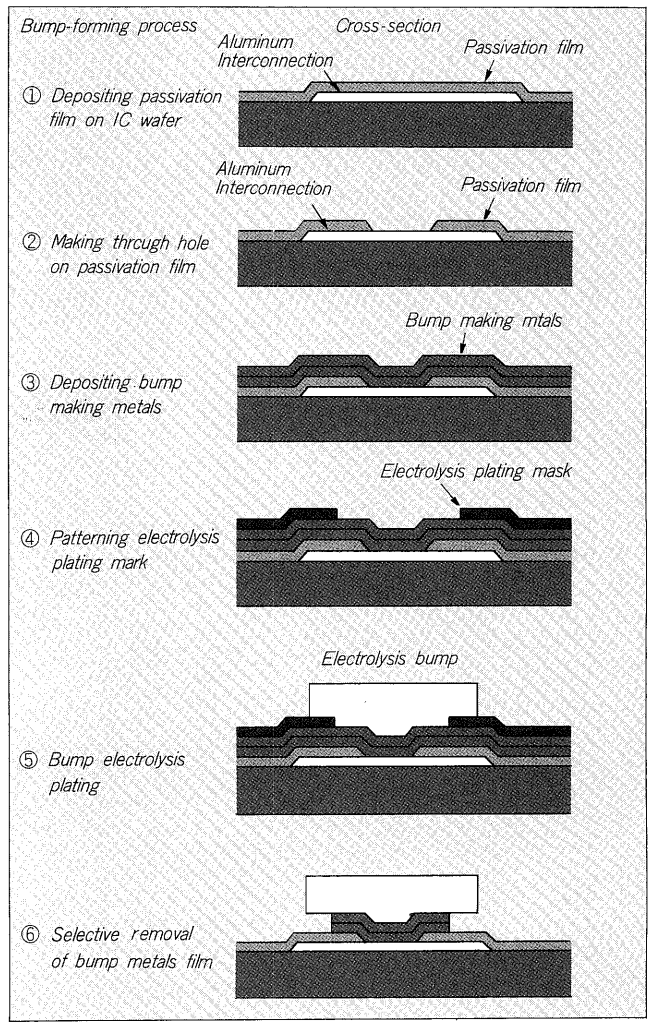
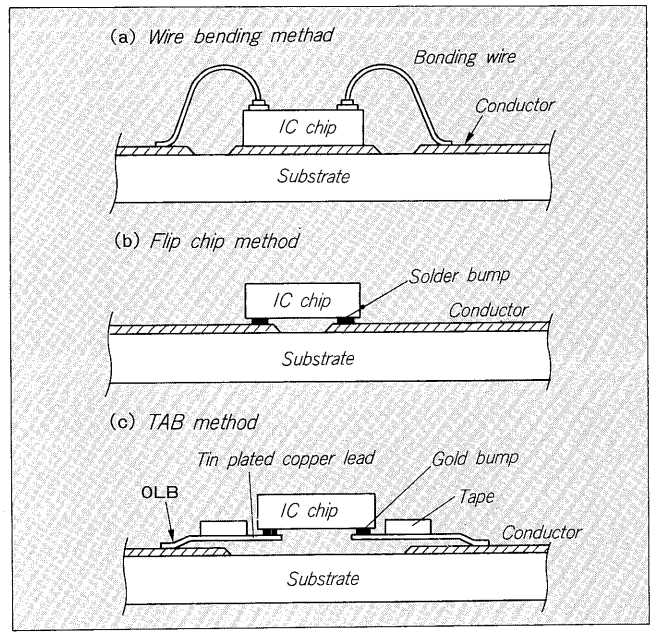


Fig. 8 Typical assembly methods



2.3 Features of the various assembly methods

The features of each assembly method are shown in *Table 1*. A comparison showing some merits of bump technology over the wire bonding method is described below.

(a) The assembly area per chip is smaller and it is possible for the assembly to have a higher density of components.
(b) Production time for the chip assembly process can be shortened.
(c) The reliability of the connection between the chip and substrate is higher.

Table 1 Comparison of the bare chip IC bonding

Item \ Method	Wire bonding	Flip chip	TAB
Electrode size	100μm□	100μmφ	70×120(μm)
Electrode pitch	170μm	180μm	90μm
Bonding intensity	5~10g/point	30~50g/point	10~20g/point
Bondability area	surroundings	whole surface	surroundings
Visibility bonding area	available	not available	available
Assembly density	△	◎	○
Reliability	○	◎	◎
Assembly cost	○	◎	◎

Notes) ◎: Very good, ○: Good, △: Normal

3. PACKAGING TECHNOLOGY

The package type and the number of terminals of IC packages made by Fuji Electric are shown in *Table 2* (pin insertion type) and *Table 3* (surface mounting type).

Table 2 The outlines and the number of terminals of pin insertion type packages.

Type	Symbol	Lead pitch length (mm)	Nominal dimensions (mils)	Number of terminals 6	8	10	14	16	18	20	22	24	28	32	40	42	44	48	52	64	68	80	84	100	120	160
Standard	DIP	2.54	300	● ○	● ○		● ○	● ○	● ○	● ○	● ○	● ○	● ○													
			400								● ○															
			600									● ○	● ○		● ○			●								
Shrink	SDIP	1.778	300									●														
			600													●										
			750																	●						

●: Plastic, ○: Ceramic DIP: Dual Inline Package, SDIP: Shrink Dual Inline Package

Table 3 The outlines and the number of terminals of surface mounting type packages

Type	Symbol	Lead pitch length (mm)	Nominal dimensions (mils)	Number of terminals 6	8	10	14	16	18	20	22	24	28	32	40	42	44	48	52	64	68	80	84	100	120	160
Flat	SOP	1.27	150*		●		●	●																		
			300*					●	●	●		●	●													
			300					●		●																
	Special SOP	1.27	–									○														
		0.8	–					○																		
	QFP	1.0	–																	●						
		0.8	–														●	●				●			●	
		0.65	–																					●		●
Leaded chip carrier	PLCC	1.27	–						●	●	●		●	●			●		●		●		●			

●: Plastic, ○: Ceramic SOP: Small Outline Package QFP: Quad Flat Package
PLCC: Plastic Leaded Chip Carrier *: JEDEC nominal dimensions

Fig. 9 Typical IC packages

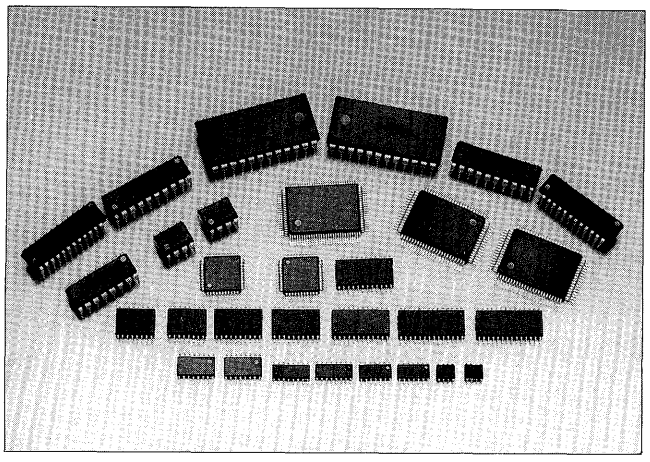
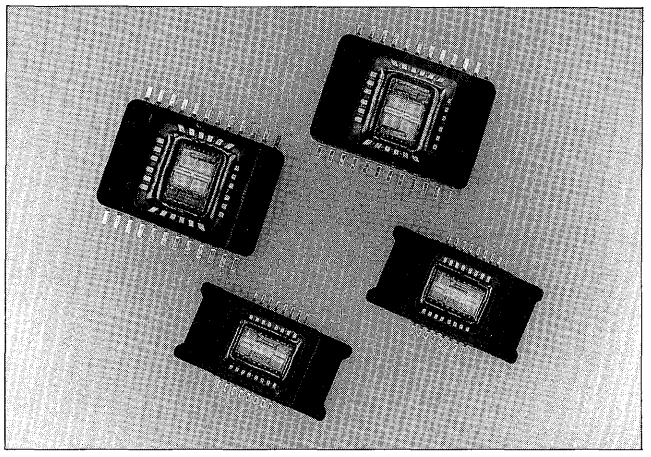


Fig. 10 SOPs for the Auto-Focus IC



External appearances of these packages are shown in *Fig. 9*.

Lead counts of Fuji's standard DIPs (lead pitch length 100 mil) ranges from 6 to 48 leads. Lead counts of Fuji's shrink DIPs (lead pitch length 70 mil) are 24 leads, 42 leads, and 64 leads.

GULL WING lead type SOPs whose leads extend in two directions out from surface mounting type packages are widely used. Fuji's SOPs are JEDEC 150 mil type, 300 mil type (JEDEC defines packages as SOPs on the basis of package body dimensions) and EIAJ 300 mil type (EIAJ defines packages on the basis of footprint center dimention values). Lead pitch length of these SOPs is 50 mil.

Special SOPs developed for the Auto-Focus IC are ceramic packages sealed with a glass lid (see *Fig. 10*).

QFPs whose leads extend in four directions out from surface mounting type packages are superior for high density mounting compared to the other molded packages. The standard lead pitch lengths of the outer leads are 1.0mm, 0.8mm, and 0.65mm, based on the concept of "fixed body variable lead pitch" where the body is fixed and the lead pitch is reduced. QFPs of 64 leads, 80 leads, and 100 leads use the same plastic body, while another type is used for QFPs of 120 leads and 160 leads.

PLCCs whose leads are bent in a J-letter shape are easier to handle than SOPs and QFPs. Lead counts of Fuji's PLCCs ranges from 18 leads to 84 leads. Lead pitch length of these PLCCs is 50 mil.

4. CONCLUSION

This paper has given an outline of characteristic production techniques, and applications as concerns ICs produced by Fuji Electric.

Year by year, developments in this field have been driven to higher levels and greater variety by demands for high density and lower cost. To realize these demands, high level technological development is made necessary to create new products. The attentive technology that is made possible in great demand.

As Fuji Electric supplies products to match these market trends, I believe the overall level of electronics will promoted and advanced.