PDP Address Driver IC Technology

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1. Introduction

PDPs (plasma display panels) have the merit of large screen size and thin design. They have improved their prior problems of insufficient brightness and contrast to achieve CRT-comparable levels, and consequently, the market for PDPs for use in household televisions is growing rapidly. Lower price is the key for PDPs to become even more popular, and lower priced driver ICs are also in demand.

Fuji Electric developed a 2nd generation address driver IC in 2001, and is presently mass-producing and supplying this chip. However, in response to demands for lower cost, Fuji Electric has recently developed process and device technologies that reduce the chip cost to 2/3 that of a conventional chip, and has applied these technologies to 3rd generation address driver IC products.

This paper presents an overview of the process and device technologies, and an overview of the 3rd generation address driver IC products that utilize these technologies.

2. Process Technology

For manufacturing address driver IC's, Fuji Electric has been applied a pn junction isolated process technology using an epitaxial wafer with a buried layer[(1)], that is high-performance and lower cost. However, in response to market demand for even lower costs, it is necessary to not only reduce the steps of wafer processing, but also to create a wafer process infrastructure capable of maintaining a stable supply even if production quantity should increase in the future.

In response to these demands, Fuji Electric has developed a new process, features of which are listed below:

(1) Wafer processing is simplified through sharing of the diffusion layer and reduction of the oxidation process, thereby enabling the number of mask steps to be reduced to 75 % that of conventional process.

(2) Adoption of 8-inch wafer process, including an epitaxial wafer process with a buried layer, to provide an infrastructure capable of maintaining a stable supply even if production quantity should increase in the future.

3. Device Technology

In order to decrease chip cost, not only must wafer process be reduced, but also the chip size must be decreased. For these 3rd generation address driver ICs, device design was optimized and the chip size was reduced to less than 70 % of the conventional size. An overview of this device technology is presented below.

3.1 High-voltage device shrinking technology

High-voltage devices occupy approximately 50 % of the total area of an address driver IC. Accordingly, the most efficient way to reduce the chip size is to shrink the size of the high-voltage devices. Figure 1 shows a cross-section of a high-voltage n-channel MOSFET (metal oxide semiconductor field effect transistor), otherwise known as HVNMOS.

HVNMOS uses a Resurf structure, but this time the trade-off characteristics between breakdown voltage and on-resistance were improved by optimizing the length (L_d) of the extended n-well that act as the drain drift region. Moreover, the channel length (L_g), and threshold voltage was optimized and device pitch was shortened. Figure 2 shows the relationship between drain current and drain voltage of the HVNMOS.

We shrinked high-voltage p-channel MOSFET

Fig.1 HVNMOS cross-section

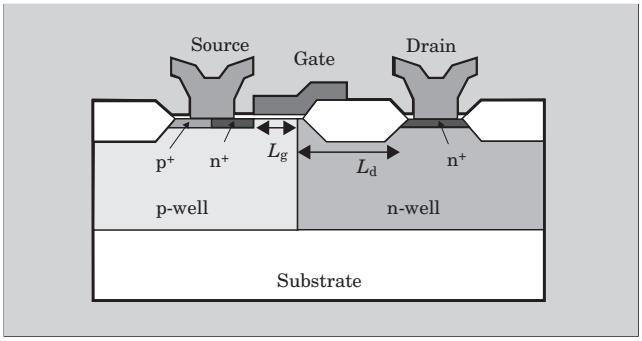


Fig.2 HVNMOS *I*-*V* characteristics

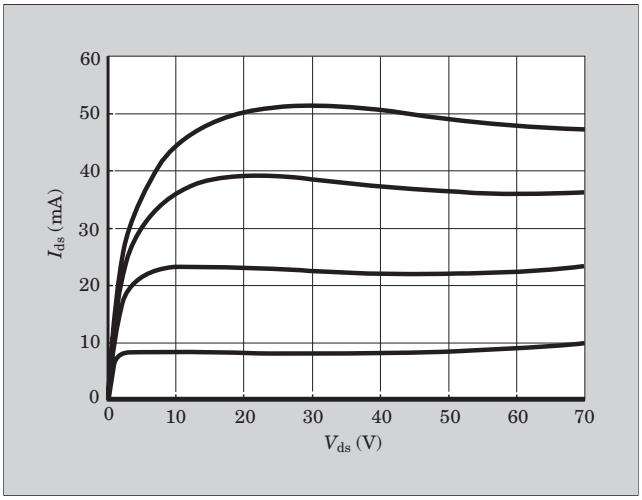


Fig.3 HVPMOS *I*-*V* characteristics

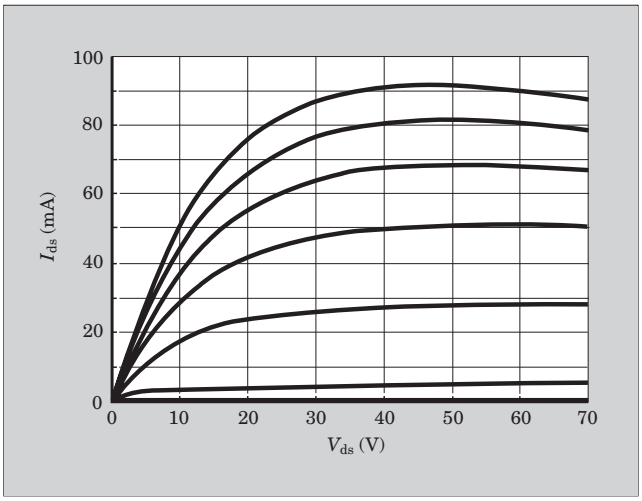
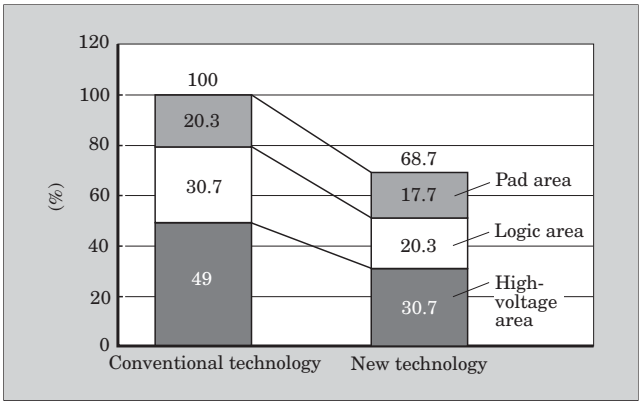


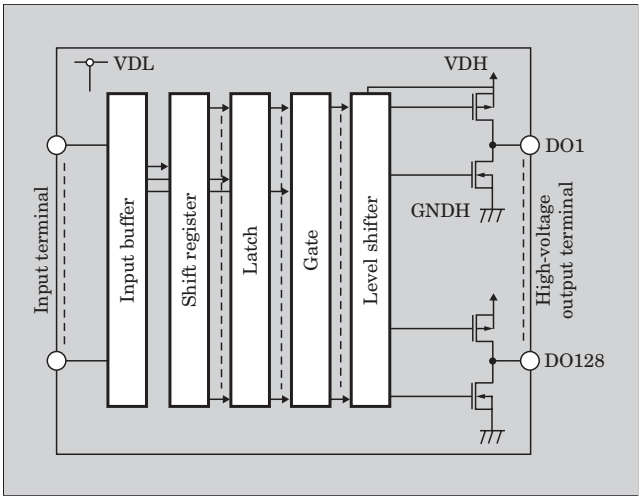
Fig.4 Device size comparison



(HVPMOS) in similar way. Figure 3 shows the *I*-*V* characteristics of HVPMOS device.

As a result of implementing this device shrinking technology, high-voltage devices capable of 70 V switching operation were realized with 60 % of the size of Fuji Electric's prior comparable devices.

Fig.5 Block diagram



3.2 Total device size comparison with conventional technology

In addition to high-voltage devices, low-voltage devices (logic area) and the pad size were also reduced.

(1) Scaled down design rules enabled shrinking of the design area to 2/3 that of Fuji Electric's conventional technology.
(2) Pad size was reduced to 90 % of the conventional one.

The above results enabled the total device size to be reduced to less than 70 % that of conventional technology (Fig. 4).

4. Application to 3rd Generation Address Driver ICs

These newly developed processes and devices were applied to the development of a color PDP address driver IC, which is introduced below.

4.1 Overview

Features of Fuji Electric's newly developed color PDP address driver IC are listed below:

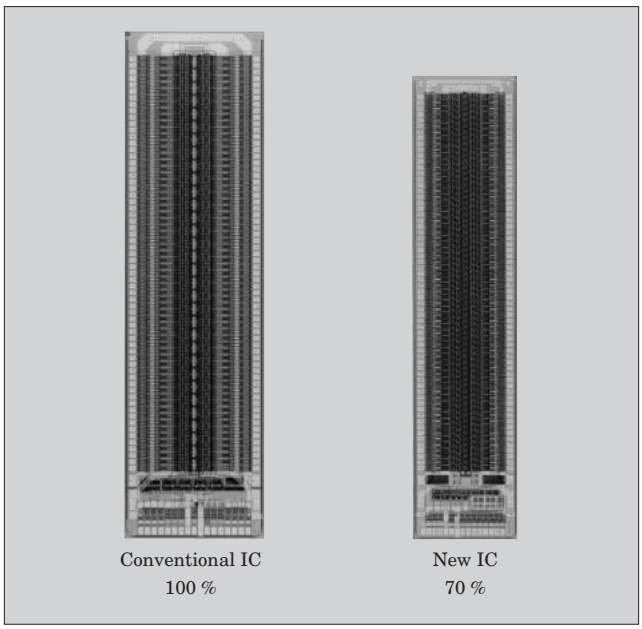
(1) 128-bit high-voltage push-pull outputs
(2) High-voltage output: 85 V (max), ±30 mA (std)
(3) High-voltage output, high switching speed
(4) High speed data transfer: 40 MHz
(5) 3.3 V CMOS input interface
(6) 4-bit data I/O port
(7) Four 32-bit bi-directional shift registers

4.2 Block diagram

Figure 5 shows a block diagram of the new IC.

The new IC consists of an input buffer circuit that enables use of a 3.3 V CMOS input interface, four 32-bit bi-directional shift registers, a 128-bit latch, a gate for controlling all H/L/Z high-voltage outputs, a low-power level shifter, and a 128-bit high-voltage push-pull output circuit.

Fig.6 Chip photograph (comparison of chip size)



4.3 Features and comparison to conventional ICs

4.3.1 Chip size

Figure 6 shows photographs of both a conventional IC chip and new IC chip, to provide a visual comparison of the relative chip sizes. By adopting newly developed low on-resistance devices and using a scaled down wafer process, this IC realizes the performance equivalent to a conventional IC, while achieving a smaller chip size which is approximately 70 % that of a conventional IC chip.

4.3.2 Typical characteristics

Table 1 shows the comparison of typical characteristics of new IC with those of conventional IC.

(1) High-voltage H/L output voltage

Characteristics comparable to those of the conventional IC were realized for both H output voltage ($V_{OH\,DO}$) and L output voltage ($V_{OL\,DO}$). Although these characteristics have a large effect on the size of a high-voltage device, the device size was reduced to approximately 60 % that of a convention device, and characteristics comparable to those of a conventional IC were realized.

(2) Current consumption during operation (logic area)

Optimization of logic circuit device parameters enabled current consumption (I_{DD}) to be decreased to approximately 55 % that of a conventional IC.

Table 1 Comparison of typical characteristics

Symbol	Condition	Conventional IC	New IC	Units
$V_{OH\,DO}$	I_{OH} = –30 mA	64.8	65.4	V
$V_{OL\,DO}$	I_{OH} = 30 mA	2.2	2.8	V
I_{DD}	When operating at 40 MHz	34.0	18.8	mA
f_{CLK}	Without load	50.0 or above	50.0 or above	MHz
$t_{p\,HL}$	C = 50 pF	55.8	46.2	ns
$t_{p\,LH}$	C = 50 pF	130.0	135.6	ns
t_r	C = 50 pF	52.3	45.3	ns
t_f	C = 50 pF	75.6	83.5	ns

Note: At the condition of,
T_j = 25°C, V_{DL} = 5 V, and V_{DH} = 70 V

5. Conclusion

This paper has presented new PDP address driver IC technology. Fuji Electric has responded to market demands for lower cost by reducing the steps of wafer processing and by shrinking the device size.

Fuji Electric intends to continue to develop high-performance, low-cost driver ICs in order to further promote and popularize PDPs.

References

(1) Meguro, K. et al. Advances of Driver IC Techniques for PDPs. IDW'02. 2002, p.733-736.
(2) Appels, A. et al. High Voltage Thin Layer Devices (Resurf Devices). IEEE IEDM. 1979, p.238-241.