Multi-output PDP Scan Driver IC

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1. Introduction

Over the past several years, driven by advances in PDP (plasma display panel) and LCD (liquid crystal display) TV technology, flat-screen TVs have rapidly become popular in the market for home-use televisions. The market had previously been divided among large-screen PDP TVs and small-screen LCD TVs, but LCD TVs have recently entered the large-screen market, and competition with PDP TVs is intensifying. Also, with the increase in terrestrial digital broadcasts, and the greater popularity of such products as game devices and DVDs (digital versatile disks), there is demand for not only larger screen displays, but also for higher picture quality, lower cost and lower power consumption.

The peripheral circuitry accounts for a large percentage of the cost of PDPs, and requests are intensifying, year after year, for lower cost driver ICs for driving the PDPs. Since the driver ICs also control the emission of light from the panel, the driver IC performance directly affects the PDP performance. Consequently, lower cost and higher performance are continuously requested of the multiple driver ICs used in a panel.

There are two types of PDP driver ICs, scan driver ICs that select scan lines and address driver ICs that select data. Fuji Electric is developing both of these types of IC drivers. This paper introduces a 96-bit scan driver IC developed with the aim of increasing brightness and reducing cost.

2. Features of PDP Scan Driver ICs

A PDP is constructed from a rare gas mixture of Ne, Xe, or the like, encapsulated between two overlapping glass panels on which are formed an electrode matrix consisting of a horizontal arrangement of sustain electrodes, for emitting, and a vertical arrangement of address electrodes, for selectively addressing display data. The intersections of the address electrodes and sustain electrodes demarcate a single PDP cell.

The cell to be displayed is selected by opposing discharges between the address electrodes and the sustain electrodes, and surface discharge is performed among the sustain electrodes. The UV rays generated by such discharge excite fluorescent material in each cell, causing light to be emitted.

Fig.1 PDP module drive circuit

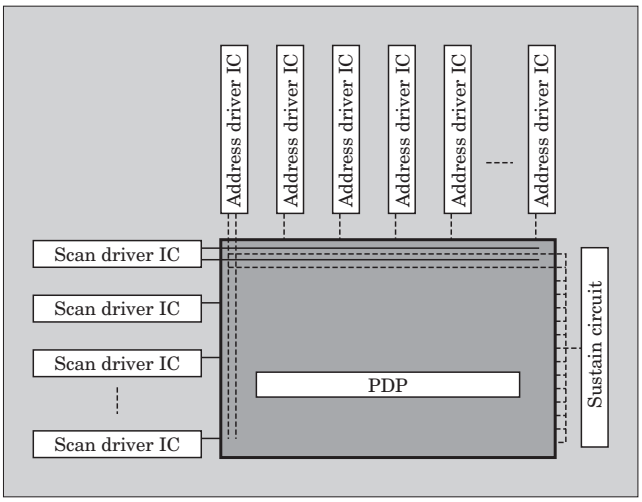


Figure 1 shows the configuration of a PDP module. Scan driver ICs drive horizontal electrodes in the panel, and simultaneously control all the discharge cells within the panel. The number of ICs used varies according to the type of the panel. Typically, a HD (high definition) panel contains at least 720 vertical pixels which configure the screen, and uses 12 conventional scan driver ICs which has 64 outputs. Also, panels having 1,920 × 1,080 pixels for displaying the intricate detail of a high vision broadcast are known as full-HD panels. A panel that supports full-HD (having at least 1,080 vertical pixels) must use 18 conventional scan driver ICs which has 64 outputs.

3. PDP Scan Driver IC Technology

3.1 Device process technology

Scan driver ICs use the SOI (silicon on insulator) method of dielectric isolation technology. Because the isolated device area can be made small without any restrictions on the device, this method is optimal in terms of cost and performance for scan driver ICs that feature a high breakdown voltage, large current and multiple outputs. In a multi-output scan driver IC, the

output circuit area occupies 50 % or more of the entire chip area, and therefore in order to reduce cost, the most effective means for reducing the IC chip area is to reduce the output circuit area. Thus, a scan driver IC which requires a large current flow uses an IGBT (insulated gate bipolar transistors) capable of a large current flow even in a small area, instead of a MOS (metal oxide semiconductor). Fuji Electric's newly developed scan driver ICs have a higher breakdown voltage than conventional scan driver ICs, and are equipped with a low ON-resistance SOI-IGBT device. The lower ON-resistance makes it possible to reduce the amount of heat generated during operation, and the higher breakdown voltage supports higher brightness.

3.2 Circuit technology

Figure 2 shows the main operation and output stage circuit of a scan driver IC. A PDP uses a reset period, an address period, and a sustain period to display a single screen. The main operation of the scan driver IC consists of address and sustain operations, and is described simply below.

(1) Reset period

In the reset period, a pulse of approximately 350 V is applied so that wall charge can be generated stably during the address period. The applied voltage causes a priming discharge to occur, and wall charge to be removed.

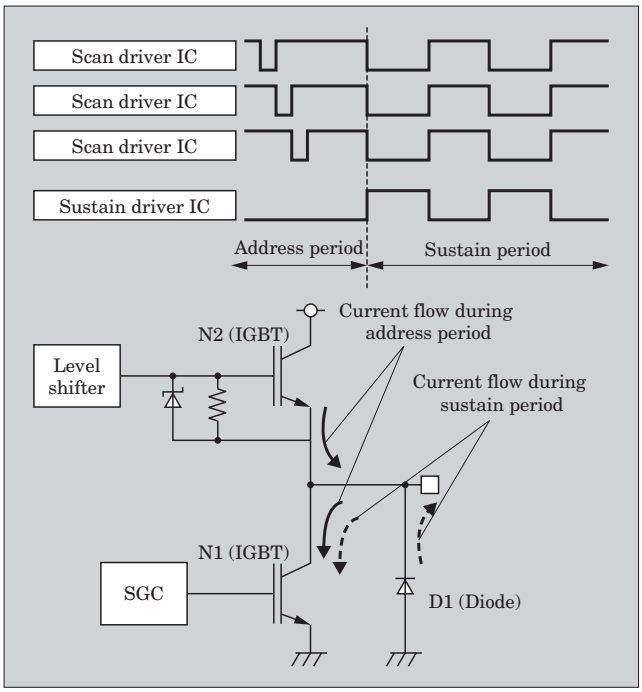
(2) Address period

In the address period, cells are selected or non-selected according to a combination of address driver IC pulses and scan driver IC pulses. When a cell is selected, N1 (IGBT) turns ON, and when de-selected, N2 (IGBT) turns ON and outputs a waveform. A selected cell flows a large current through N1 (IGBT) and performs a preliminary discharge. At this time, a voltage of approximately 70 V is applied to the address driver ICs, and for each scan line, a current of at least 1 A flows to a scan driver IC.

(3) Sustain period

In the sustain period, a voltage of approximately 180 V is applied alternately to the sustain circuit, and the repeated application of pulses causes cells selected during the address period to sustain their discharge. The discharge current is supplied from both N1 (IGBT) and D1 (diode), and a gradated display is implemented according to the number of repeated discharges.

Fig.2 Scan driver IC operation

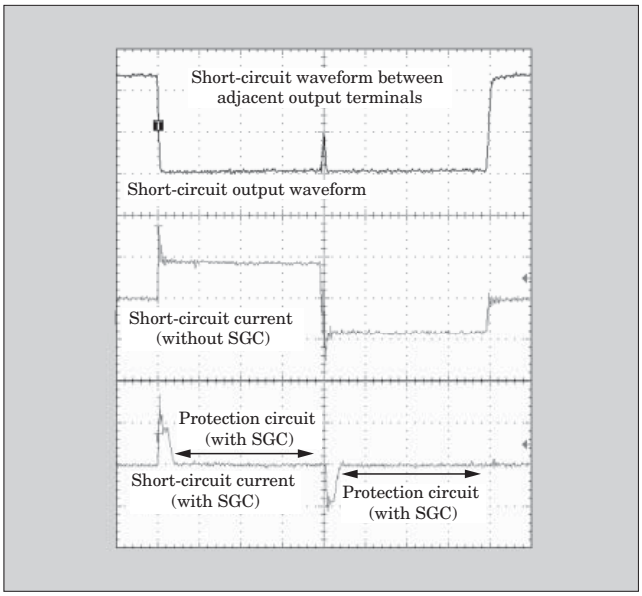


3.3 Smart gate control (SGC) technology

A problem associated with IGBTs is that if a large current is output continuously, latch-up may occur and cause the device to become damaged. In particular, in order to reduce cost, if a device is shrunk and the current density increased, then the device becomes susceptible to damage. One conceivable cause would be an abnormal discharge due to an overload short-circuit condition or abnormal operation such as in the case of short-circuited output terminals. Modifying a device so that there will be no damage when an abnormal operation occurs results in a larger device area and higher cost. Therefore, a SGC (smart gate control) circuit, capable of outputting a large current during a discharge period when current is needed and limiting the current during a discharge period when current is unnecessary, was designed and used in practical applications[1]. Since the SGC operation is controlled synchronously with a clock signal, the control circuits can be shared for a multi-output device and the control circuits can be miniaturized.

Figure 3 shows waveforms in the case where adja-

Fig.3 Short-circuit waveforms between adjacent output terminals



cent output terminals have been short-circuited. During a short-circuit condition in the case where SGC technology is not utilized, current will continue to flow and the heat generated as a result of the increased duration of the short-circuit and the rise in voltage will cause damage. However, in cases where SGC technology is utilized, the current flow is stopped after a fixed time has elapsed, and therefore if the short-circuit has a long duration, damage will not occur even if the voltage rises up to a certain level, and therefore, the current density of the device can be increased to reduce the device size. The SGC makes it possible to extend the time until short-circuit damage occurs, and by switching the device OFF before the occurrence of short-circuit damage, a short-circuit will not cause any damage to occur.

4. Application to a PDP Scan Driver IC (FD3298F)

As PDP TVs achieve larger screen sizes, higher resolution and lower cost, driver ICs are being requested to have higher breakdown voltage, larger current and lower cost. In response to these requests, and focusing on multi-output capability, Fuji Electric has increased the breakdown voltage without increasing the device size to develop a 96-bit scan driver IC that enables the number of scan driver ICs used to be reduced, from 12 (previously) to 8, in a HD panel as shown in Table 1. Also, in a full-HD panel, cost reductions can be realized by reducing the number of ICs used from 18 64-bit ICs to 12 96-bit ICs. Fuji Electric's 96-bit scan driver IC, FD3298F, is introduced below.

4.1 Features

Main features of the FD3298F are listed below.

(1) 96-bit bi-directional shift register (with 15 MHz clear function)
(2) 180 V absolute maximum rating (supply voltage for output), 7 V absolute maximum rating (supply voltage for logic)
(3) Power output supply voltage: 30 V to 150 V
(4) 5 V supply for logic
(5) Driver output current: −0.4 A/+1.4 A (source/sink)
(6) Diode output current: −1.4 A/+1.2 A (source/sink)
(7) 128-pin TQFP with exposed pad (E-PAD)

4.2 Circuit configuration

Figure 4 shows a block diagram of the FD3298F. The circuit is configured from a 96-bit bi-directional shift register circuit, a 96-bit latch circuit, data select circuits, and a 96-bit output circuit. So that the output circuit can charge and discharge the discharge cells in the panel, a totem pole output circuit configured from two devices having a high breakdown voltage is used in the output circuit. In order to prevent malfunction, Schmitt circuits are connected to the shift register input terminals, with the exception of the A/B signal terminal that determines the direction of the shift register. Also, the logic output is a trailing edge output with respect to the clock signal.

Table 1 Number of scan driver ICs used

Resolution	Scan lines	64ch IC use number	96ch IC use number
SD (VGA)	480	8	6
HD (XGA)	over 720	12	8
Full HD	1,080	18	12

4.3 Comparison with a conventional IC

Figure 5 compares the chip size of a conventional

Fig.4 FD3298F block diagram

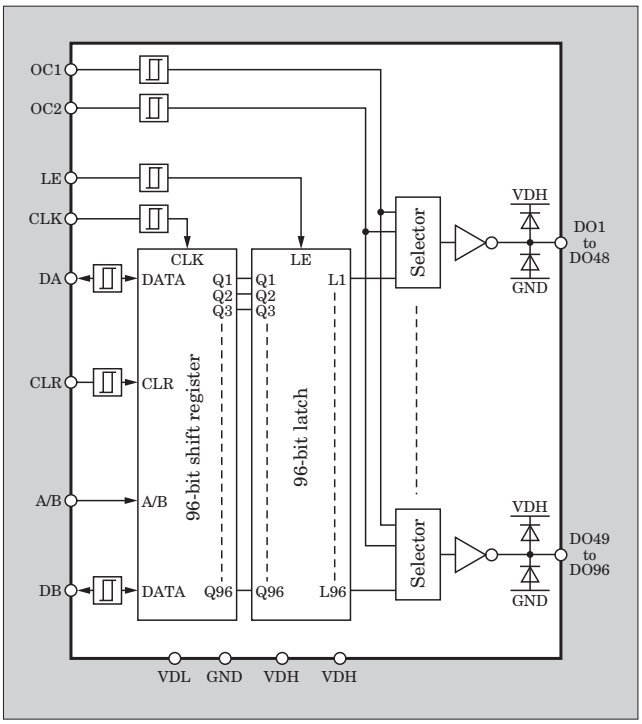


Fig.5 Die size comparison of FD3298F and conventional scan driver IC

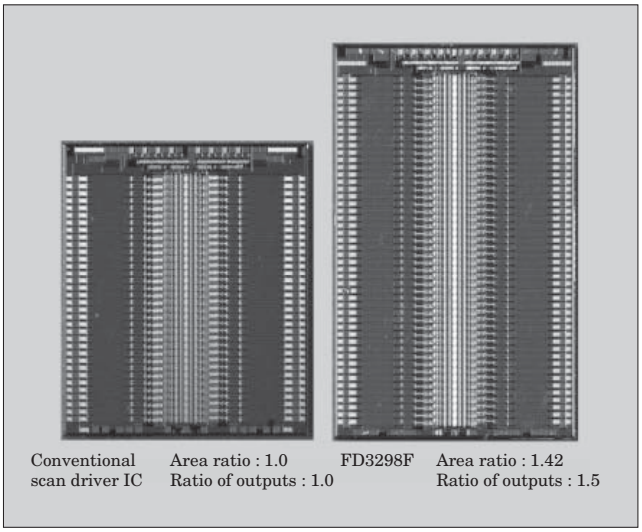
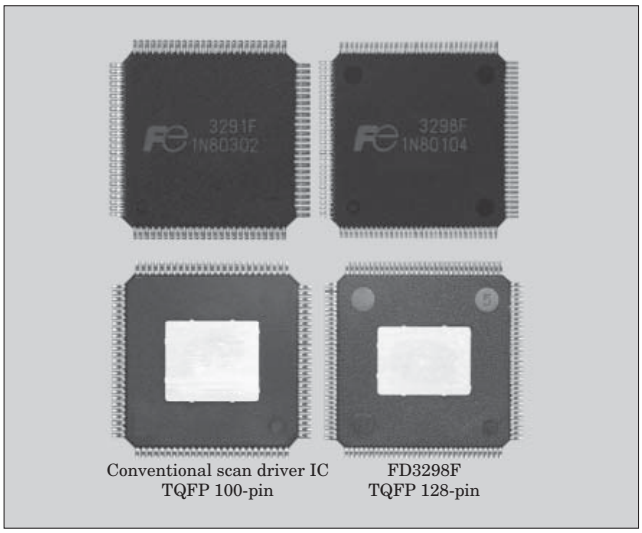


Fig.6 External appearance of FD3298F and conventional packages



scan driver IC and the FD3298F. The chip size of the FD3298F is 1.42 times that of a conventional 64-bit scan driver IC, but the number of bits is 1.5 times greater, and since the number of chips used will decrease, the cost will lower than in the case of conventional scan driver ICs.

Figure 6 shows the external appearance of the package. The conventional IC package uses a TQFP 100-pin (E-PAD) package, but since the FD3298F has a 96-bit output, the FD3298F uses a TQFP 128-pin (E-PAD) package. The increase in the number of output bits creates a problem of more heat generated, but by reducing the ON-resistance to a value lower than that of the conventional scan driver IC, the generation of heat during operation is reduced, and by increasing the number of E-PADs and pins, heat is dissipated more efficiently from the package.

5. Conclusion

Fuji Electric's PDP scan driver IC, FD3298F, which was developed with the aim to achieve higher breakdown voltage and lower cost has been introduced.

Fuji Electric intends to continue to develop device technology, circuit technology and process technology for scan driver ICs in response to marketplace and panel manufacturer's requests.

Reference

(1) Kobayashi, H. et al. PDP Scan Driver IC with Smart Gate Controlled IGBTs. IDW'04. PDP3-3.