High-Voltage CMOS Process Technology

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1. Introduction

Fuji Electric has developed processes to fabricate ICs. The process satisfies demands for a display driver IC of up to about 100V for a liquid crystal display (LCD), plasma display panel (PDP) and vacuum fluorescent display (VFD). The power control IC has up to about 40V of high voltage and high current analog signal control.

The ICs are fabricated using the CMOS (complementary MOS) oxide isolation process for driving the LCD, the junction isolation process for driving the PDP and the bipolar process for the power supply.

Besides small size and light weight, there are demands for reduced power consumption for longer battery life for electronic apparatus and devices, especially for the handy type.

An IC used in electronic apparatus and devices, small chip size by using scaling down process, variety of functions to reduce number of parts, low power consumption and low cost are demanded. The CMOS process which uses oxide isolation technology is low in cost when compared with the DMOS (double diffused-MOS) process and bipolar process of junction isolation technology. Also it is favorable for high integration because CMOS process is suitable for scaling down. Fuji Electric has developed devices using the CMOS oxide isolation process for the IC applying to driving LCD, driving PDP and power supply control.

This paper will present a summary of the process and characteristics of the device. The process enables high voltage devices of 30V, 60V and 120V to use the CMOS oxide isolation process.

2. Outline of the Process

Table 1 shows an outline of three processes. One advantage is a simple process based on the logical 1μm rule and another is the possible mounting of the high voltage and logic devices on one chip. These devices can select the process or device depending on the voltage used by the products. Fuji Electric has prepared three high voltage devices of 30V, 60V and 120V for the absolute maximum rating voltage.

Table 1 Classification of CMOS process

Process technology		Geometrical design rules	Absolute maximum ratings for voltage	Polysilicon layer	Metal layer
Polysilicon-gate-CMOS	CMOS Ⅰ	1μm	30V	2 layers	2 layers
	CMOS Ⅱ		60V	2 layers	2 layers
	CMOS Ⅲ		120V	1 layer	1 layer

Table 2 Fabrication process sequence for component device

Process flow	CMOS Ⅰ	CMOS Ⅱ	CMOS Ⅲ
n-well diffusion	○	○	○
p-well diffusion	○	○	○
p-offset diffusion	○	○	○
n-offset diffusion	○	○	○
p-guardring diffusion	○	○	
n-guardring diffusion		○	
Field oxidation	○	○	○
First gate metallization	○	○	○
Second gate metallization	○	○	
Source/drain diffusion	○	○	○
Contact window etching	○	○	○
First interconnections metallization	○	○	○
Second interconnections metallization	○	○	
Passivation film deposition	○	○	○

Table 2 shows the process flow. The process flow for the logic device is identical to the other devices and the addition or elimination of optional flows for high voltage and bipolar devices is possible.

3. Component Devices

Characteristics of each device are shown in Table 3.

Fig.1 Schematic cross section of component devices

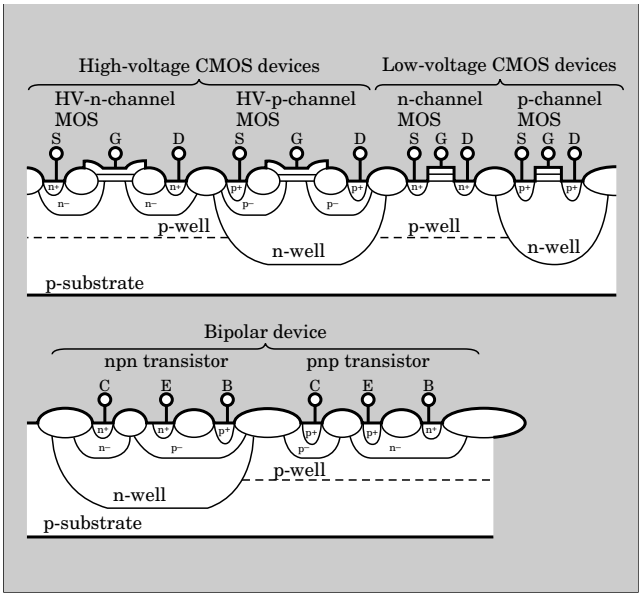


Fig.2 Equipotential plots for the 30V class CMOS device

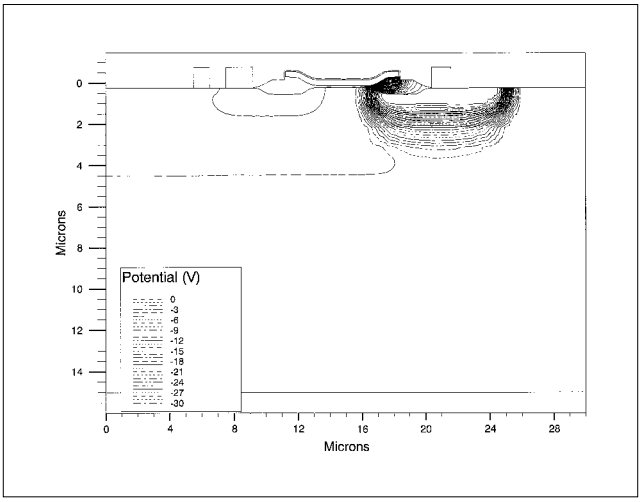


Table 3 Characteristics of component devices

Devices		Characteristics	1μm rule CMOS process		
			CMOS Ⅰ	CMOS Ⅱ	CMOS Ⅲ
CMOS	Low-voltage n-channel MOSFET	V_{th} (V)	1.0		
		BV_{dss} (V)	12.0		
	Low-voltage p-channel MOSFET	V_{th} (V)	− 1.0		
		BV_{dss} (V)	− 12.0		
	High-voltage n-channel MOSFET	V_{th} (V)	1.5	2.5	1.0
		BV_{dss} (V)	65.0	80.0	160.0
	High-voltage p-channel MOSFET	V_{th} (V)	− 2.0	− 3.5	− 1.0
		BV_{dss} (V)	− 55.0	− 75.0	− 160.0
Bipolar	npn transistor	h_{FE}	90.0	—	—
		BV_{ceo} (V)	18.0	—	—
	pnp transistor	h_{FE}	35.0	—	—
		BV_{ceo} (V)	80.0	—	—
	Zener diode	V_z (V)	7.5	—	—

3.1 High-voltage CMOS device

Figure 1 shows a cross section of the high voltage CMOS device. Under the high voltage biased between source-drain electrode of CMOS device, punch-through effect, impact ionization, hot-carrier are observed due to the high electric field around the drain region. Punch-through effect reduces the break-down voltage and impact ionization and hot-carrier cause reduction of reliability.

Then, in order to reduce the high electric field of the CMOS, a well-known structure of connected high-concentration diffused layers of the source and drain with a low-concentration diffused layer are adopted. With the low-concentration diffusion layer, the electric field around the drain is lowered, and the breakdown voltage of the device is increase and generation of the hot-carrier is reduced. Figure 2 shows equipotential plots near the drain region in the 30V class device using a two dimensional simulator (ATLAS).

According to the required breakdown voltage of the device, the CMOS has designed to obtain a maximum current while satisfying high voltage by optimizing parameters such as channel length, concentration and depth of the lightly doped diffusion layer and gate oxide thickness.

Figures 3 through 8 show current-voltage characteristics of the high voltage devices.

3.2 Bipolar device

In order to apply the device to a high precision analog circuit, the process flow of the 30V class CMOS has included the production process for the npn transistor, pnp transistor and zener diode as options.

The process cost of these devices can be reduced by using the common use of both the high voltage process sequence.

3.3 Low-voltage device

The low-voltage device has been designed commonly in every process and used as a common device. The design attempted to micronize the device by using the 1μm rule. The IC with higher integration and speed has been realized.

4. Application

Figure 9 shows a photograph of a power control IC chip fabricated by the 30V class CMOS process.

Fig.3 I_d-V_d characteristics of the 30V class n-channel MOSFET

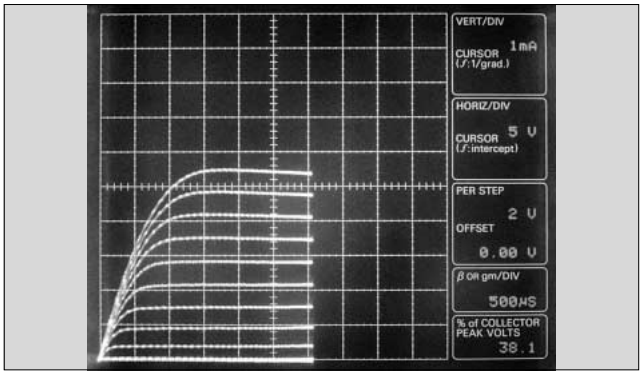


Fig.4 I_d-V_d characteristics of the 30V class p-channel MOSFET

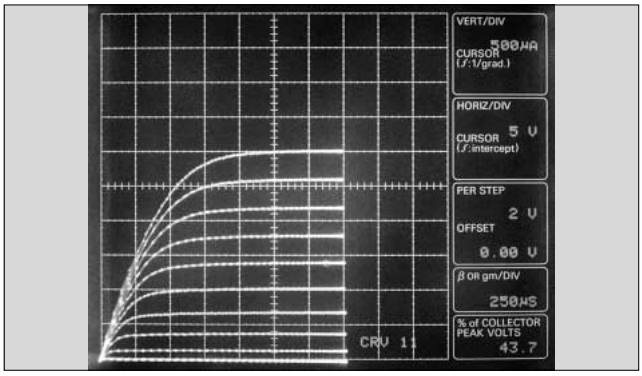


Fig.5 I_d-V_d characteristics of the 60V class n-channel MOSFET

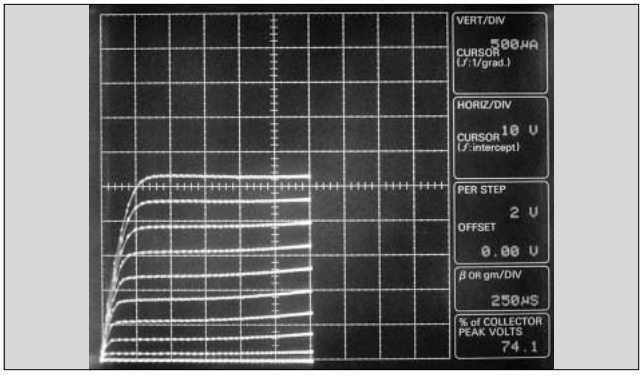


Fig.6 I_d-V_d characteristics of the 60V class p-channel MOSFET

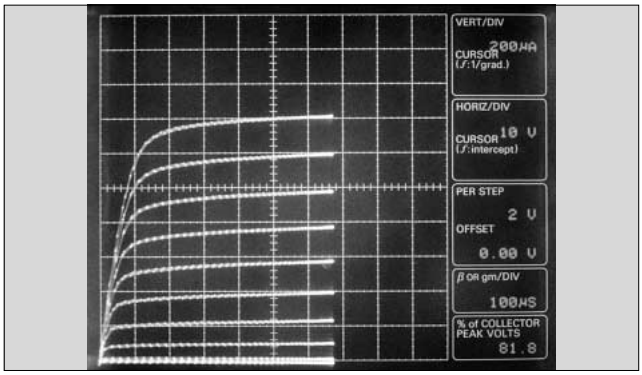


Fig.7 I_d-V_d characteristics of the 120V class n-channel MOSFET

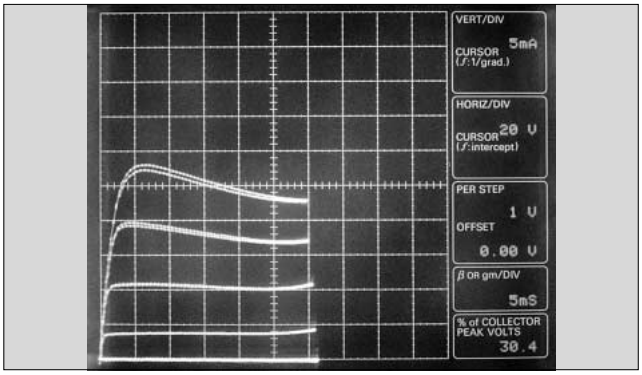


Fig.8 I_d-V_d characteristics of the 120V class p-channel MOSFET

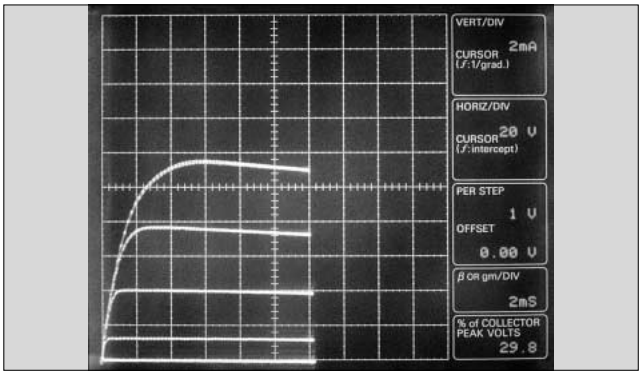
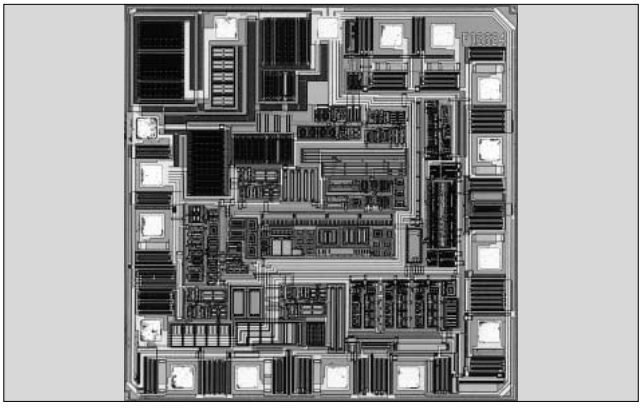


Fig.9 An IC chip fabricated by the 30V class CMOS process



5. Conclusion

This paper introduced the process flows and devices that enable the mounting bipolar device, logic device, and high voltage CMOS devices up to 120V on one chip. All devices are based on the 1μm rule CMOS.

In the future, we will develop micronized process using high voltage device technology and contribute to social requirements by supplying such devices as systematization, small size and lower power consumption.