Development of SiC Bipolar Devices Using Simulation

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ABSTRACT

In SiC (silicon carbide) devices, which are wide band-gap semiconductors, bipolar devices are considered beneficial for achieving a high withstand voltage in excess of 13 kV. Fuji Electric has improved prediction accuracy by repeatedly adjusting parameters based on the analysis of differences between simulation predictions and actual results. We implemented withstand voltage characteristic simulations, forward characteristic simulations, and switching characteristic simulations, and then reflected the measured physical property values into the parameters, while also taking into account interface charges and parasitic resistance. As a result, we were able to reproduce with a high level of accuracy the characteristics of actual devices.

1. Introduction

In recent years, wide band-gap semiconductors have started to be put to practical use as semiconductors for power devices, replacing conventional silicon (Si) ones. Wide band-gap semiconductors can offer device characteristics of a high withstand voltage and low resistance because they have a low intrinsic carrier concentration and do not produce a leakage current easily unless a higher temperature/electric field than that which causes Si to do so is applied. Table 1 shows the physical property values of major wide band-gap semiconductors[1]. For silicon carbide (SiC) devices, in particular, materials and constituents have been improved through research and development for many years. Some unipolar devices have already been commercialized, including Schottky barrier diodes and transistors (metal-oxide-semiconductor field-effect transistor [MOSFET], junction field-effect transistor [JFET]). On the other hand, bipolar devices, which have excellent properties as large-current high-withstand-voltage devices, are still in the stage of research and development. This is because some issues remain regarding the characteristics and processes of p-type semiconductors used as a supply source of hole carriers, and the problem of degradation promoted by the recombination of holes and electrons has not been solved yet.

Table 1 Physical property values of wide band-gap semiconductors

Item	Wide band-gap semiconductor				Si
	3C-SiC	4H-SiC	6H-SiC	GaN	
Band-gap (eV)	2.36	3.26	3.02	3.42	1.12
Electron mobility (cm^2/Vs)	1,000	1,000	450	1,500	1,350
Hole mobility (cm^2/Vs)	100	120	100	150	600
Dielectric breakdown strength (MV/cm)	1.4	2.8	3.0	3.0	0.3
Saturated drift velocity (cm/s)	2.0×10^7	2.2×10^7	1.9×10^7	2.4×10^7	1.0×10^7
Thermal conductivity [W/(cm·K)]	4.9	4.9	4.9	2.0	1.5
Baliga's figure of merit*	62	495	274	1,128	1

* Baliga's figure of merit is a figure of merit for unipolar devices proposed by Baliga. It is an indicator of the limitation characteristics determined by materials.

By using simulations to predict ideal characteristics and comparing them with the result of actual measurement, we can identify problems in the devices and make use of them for improvement. The accuracy with which various physical property parameters and process dependence can be identified has also been improved by fitting data between the simulation and the result of measuring electrical characteristics using prototypes.

2. SiC Bipolar Devices

The research and development of bipolar devices which allow large-current operations, such as SiC-PiN diode or SiC insulated-gate bipolar transistor (SiC-IGBT), has continued since 2009 at the National Institute of Advanced Industrial Science and Technology. This R&D is part of the Tsunenobu KIMOTO project of the Funding Program for World-Leading Innovative R&D on Science and Technology (FIRST). Fuji Electric has also been participating in

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this project since the beginning. Bipolar devices require a bias voltage higher than the built-in voltage related to the band gap for forward operation, and SiC requires 2.5 V or higher. Although unipolar devices have high resistance, they have no built-in voltage. Consequently, bipolar devices are expected to have advantages in terms of conduction loss probably in a high-voltage region where the withstand voltage exceeds 5 kV. Figure 1 shows examples of structural cross-sectional views of a PiN diode and an n-type IGBT. Figure 2 shows photos of the prototypes of an n-type IGBT chip and wafer.

From the beginning, FIRST set 13-kV-class devices as a target, developed an n-type IGBT with target specifications of a 13-kV withstand voltage, 11 mΩcm^2 characteristic differential on-resistance, 8 × 8 mm^2 chip size and 60 A per chip, and confirmed the switching operation at 6 kV.

In order to obtain a withstand voltage exceeding 10 kV, even SiC devices which can provide a high-withstand voltage require a low impurity concentration layer of 150 µm or more. Unlike Si, there is no SiC substrate with a low impurity concentration. One of the methods of creating a substrate is the sublimation method that sublimates SiC powder material at the extremely high temperature of 2,000 °C or more to grow a layer on a seed crystal. Unfortunately, the substrates created by this method cannot avoid being contaminated with the surrounding materials. Hence, it is impossible to keep impurities to 1 × 10^{16}/cm^3 or less, which is required of high-withstand voltage devices. PiN diodes use wafers on which a low-impurity-concentration layer is epitaxially grown on an n-type substrate with a CVD device. On the other hand, there is no p-type substrate for n-type IGBTs that has a low defect density applicable to creating devices. As a countermeasure, they create a substrate by epitaxially growing a low-concentration n layer of 150 µm or more on an n-type substrate and then a high-concentration p layer of approximately 200 µm on it, and scraping off the n-type substrate completely. Due to the use of thick epitaxial layers having different types of impurities and concentration levels, the presence of a certain amount of defects that cause degradation is inevitable. There are problems of not only the person-hours required for substrate manufacturing, but also the frequent breakage of substrates due to large warpage and high stress, resulting in an insufficient number of prototypes.

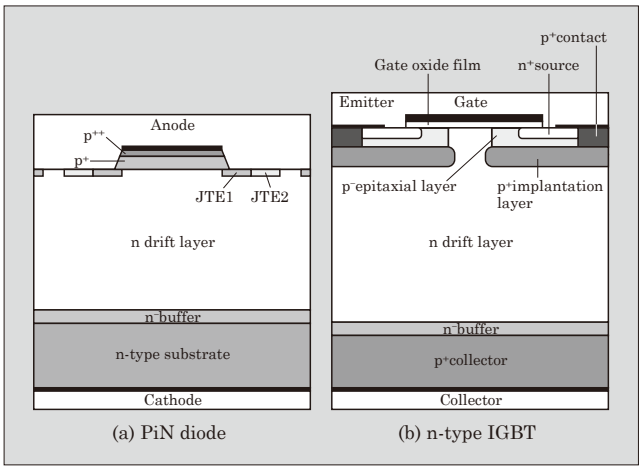

Fig.1 Examples of structural cross-sectional views of PiN diode and n-type IGBT

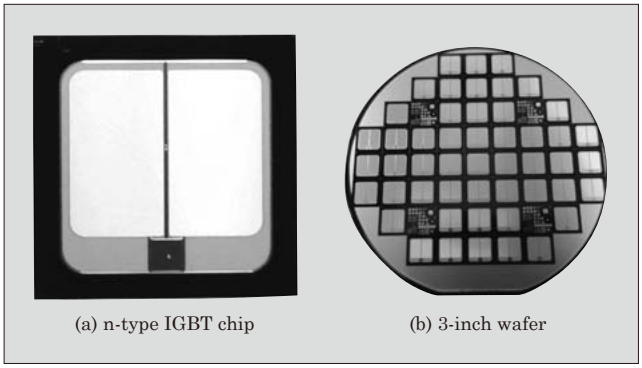

Fig.2 Prototypes of n-type IGBT chip and wafer

3. Simulation Using Ultra-High-Withstand Voltage Bipolar Devices

3.1 Challenges in simulation

Since the number of prototypes for development is limited, it is effective to use device simulation to consider a preliminary design. Unfortunately, the accuracy of the parameters for conducting a simulation is imperfect compared with the case of Si. The characteristics concerning p-type semiconductors, in particular, often show lower performance than the ideal values, and greatly depend on the processes specific to manufacturing lines. Table 2 shows major causes for simulation errors of ultra-high-withstand voltage bipolar devices. We improved the prediction accuracy by analyzing the differences between the results of the simulation prediction and actual measurement and repeatedly correcting the parameters.

The simulation of wide band-gap semiconductors uses more bits than usual for a floating point calculation because it is necessary to improve the calculation accuracy so that low leak current characteristics can be

Table 2 Major causes of simulation errors

Item		Cause
Related to p-type semiconductor	Low ionization rate	Deep Al impurity level
	Low activation rate	Damage or low recovery from ion implantation
	High contact resistance	Immature silicide electrode process
Related to thick epitaxial film	Low mobility	Existence of defect/downfall
	Low lifetime	The process centers on recombination resulting in the existence of defects of density in the order of 10^{12} to 10^{13}/cm^3.

handled. Consequently, the calculation tends to take longer. In order to improve convergence, carrier concentration is enhanced artificially with heat and light excitation and calculations are performed within the range where the actual withstand voltage is not affected.

3.2 Simulation of withstand voltage characteristics

Several institutions have reported the electric field dependence of an impact ionization coefficient that greatly affects withstand voltage calculations, including doping density dependence and temperature dependence[1]. The currently used SiC has a configuration of a hexagonal crystal system called 4H, and is anisotropic in terms of mobility and an impact ionization coefficient. There have been reports on the use of an anisotropic impact ionization model that defines a value in the direction of the <0001> axis and a value in the direction perpendicular to the axis individually. It is suggested this would improve the accuracy of the withstand voltage simulation at the device termination section where the electric field in the direction perpendicular to the <0001> axis is important[2].

Figure 3 shows a diagram of the termination structure of a 13-kV n-type IGBT. In order to mitigate the horizontal electric field intensity at the termination section, the junction termination extension (JTE) forms a p-type impurity layer. To achieve an ultra-high-withstand voltage, we provided JTE sections with 2 different levels of concentration. The JTE has a length of 500 µm, providing an extremely short termination structure compared with high-withstand-voltage Si devices. In order to achieve a structure with a high withstand voltage, it is necessary to adjust the JTE concentration so that the electric field intensity from the inside to the outside of the JTE is uniform.

As stated above, you cannot use n-type SiC substrates directly to create n-type IGBTs, and so experimental prototyping of many number of substrates is difficult. On the other hand, PiN diodes can be created with n-type substrates and it is relatively easy to prepare substrates for experimental prototyping. Consequently, we started experimentally prototyping high-withstand-voltage devices from PiN diodes. Figure 4 shows the JTE dose dependence of the withstand voltage in a PiN diode. It shows the predicted

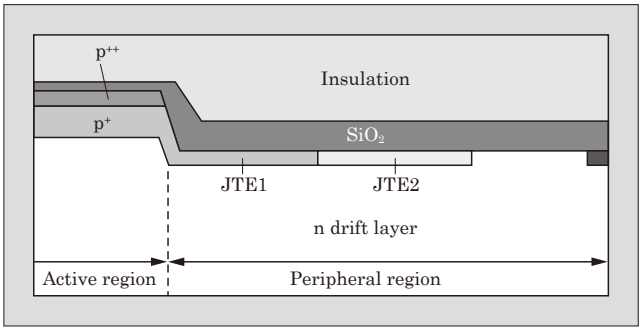

Fig.3 Diagram of termination structure of 13-kV n-type IGBT

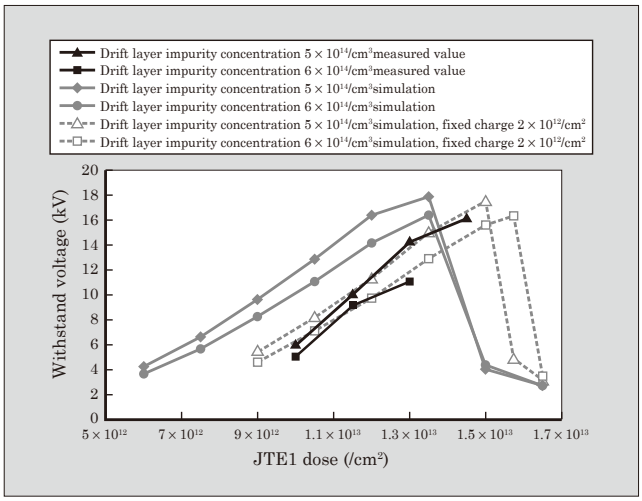

Fig. 4 JTE dose dependence of withstand voltage in PiN diode

values of the simulated withstand voltage and the results of measuring a prototype of PiN diodes in which impurity concentration levels in the drift layer are $5 \times 10^{14}/cm^3$ and $6 \times 10^{14}/cm^3$. The JTE dose on the X axis represents the total amount of impurities per unit area which is ion-planted to the JTE section; and the Y axis represents the withstand voltage.

The withstand voltage values tend to become higher as the JTE dose increases; however, the values of the simulation prediction and actual measurement do not coincide. This PiN diode has anode electrodes formed on the SiC carbon face (C-face) as in the case of IGBTs, so that the p-type JTE region of the termination section is also formed on the C-face. MOS capacity measurement has suggested the existence of a large quantity of interface charges on the interface between the p-type SiC and oxide film. These interface charges may have some influence on the withstand voltage. Figure 4 is the result of the withstand voltage simulation in which positive charges are placed on the interface. We found that the measured value and simulation prediction value coincide when approximately $2 \times 10^{12}/cm^2$ of positive charges exist.

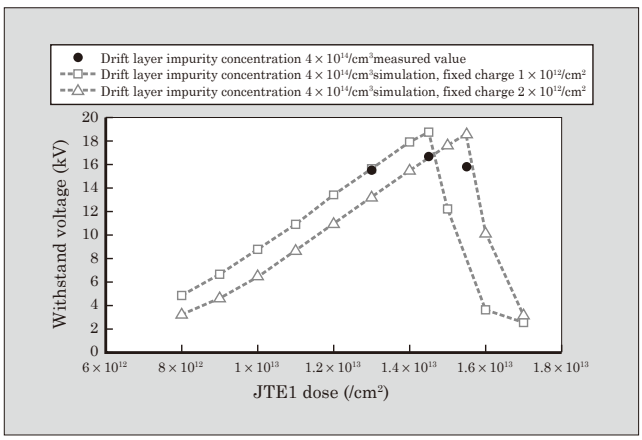

Fig.5 JTE dose dependence of withstand voltage in n-type IGBT

Figure 5 shows the JTE dose dependence of the withstand voltage in an n-type IGBT. It compares the predicted withstand voltage value and the withstand voltage of actual measurement of an n-type IGBT. In an IGBT, holes flow in through the p-type collector on the back side. Consequently, a drop of several kV in the withstand voltage is expected compared with the case of PiN diodes. By applying the prototyping result of the device for a PiN diode withstand voltage evaluation and adjusting the JTE dose in advance considering the amount of fixed charges, we obtained a target withstand voltage that exceeds 13 kV.

3.3 Forward characteristics simulation

Simulating the forward characteristics of bipolar devices requires actual mobility and lifetime of electrons and holes. For a thick n-type drift layer exceeding 150 µm, the ideal lifetime is 10 µs or more; however, the current lifetime remains at several µs or less. The $Z_{1/2}$ center, which is the typical point defect of SiC, is said to be the killer level making the lifetime shorter. A report suggests that p-type semiconductors have a specific killer level resulting from the point defects related to Al acceptors. It is considered that this level may also have an influence on bipolar devices. Predicting the hole implantation amount requires the activation rate and ionization rate of the p-type layer. The activation rate of the impurities in an epitaxially grown p-type layer is almost 100%, whereas in the case of ion implantation, the activation rate greatly depends on the process. Moreover, Al acceptors, which are the source of hole carriers, exist in a deep level so that their ionization rate at room temperature is low. Due to imperfect accuracy of the temperature, concentration and process dependence in the parameters including lifetime, ionization rate and activation rate, the accuracy of predicting the forward characteristics is insufficient.

Figure 6 shows the forward characteristics of a 13-kV PiN diode. It compares the I-V waveforms of the simulation and actual measurement result of the PiN diode using a p-type epitaxially grown layer as an anode at room temperature and 200 °C. The characteristics in the minute current range near the built-in voltage that is dependent on the band gap are close to and coincide well with the ideal values. In the large-current region, however, the measured forward voltage V_{on} is higher and indicates higher resistance than that in the ideal state. It is expected that the inclusion of large-resistance components is caused by the fact that the current increased linearly instead of exponentially with the bias voltage.

A p-type SiC tends to have higher contact resistance with the electrode than that of an n-type SiC. And it can be thought that this diode has a high contact resistance in the order of $10^{-2}\,\Omega cm^2$ at room temperature. Although measurement using the transfer length method (TLM) showed a contact resistance in the order of $10^{-3}\,\Omega cm^2$, an actual device seems to have several times higher resistance. Another institution has also reported an example of improved forward characteristics when the electrode formation process was improved to reduce contact resistance. We can expect characteristics to be improved when processes are improved.

The forward voltage of a SiC PiN diode drops at a high temperature. This is because the lifetime becomes longer by several times at a high temperature and the higher ionization rate of Al impurities promotes a better contact resistance and hole carrier injection. The longer lifetime seems to be caused by the fact that the influence of the $Z_{1/2}$ center forming the major killer level decreases at a higher temperature. By considering these factors and applying them to the temperature dependence of the lifetime and contact resistance, we could reproduce the forward characteristics at 200 °C. Figure 7 shows the forward characteristics of a 13-kV n-type IGBT. It compares the results of measurement and simulation of the 13-kV n-type IGBT prototype. This IGBT has the same gate structure as the implantation and epitaxial MOSFET (IEMOS) of the National Institute of Advanced Industrial Science and Technology. Consequently, we estimated its forward characteristics by applying the channel mobility of the IEMOS and the parameters of the PiN diode. It can be thought that a higher operat-

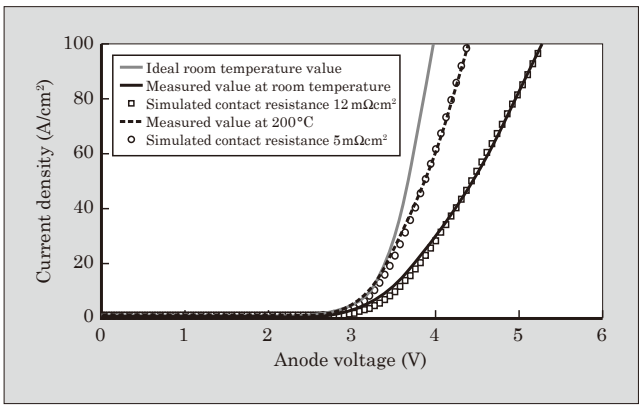

Fig.6 Forward characteristics of 13-kV PiN diode

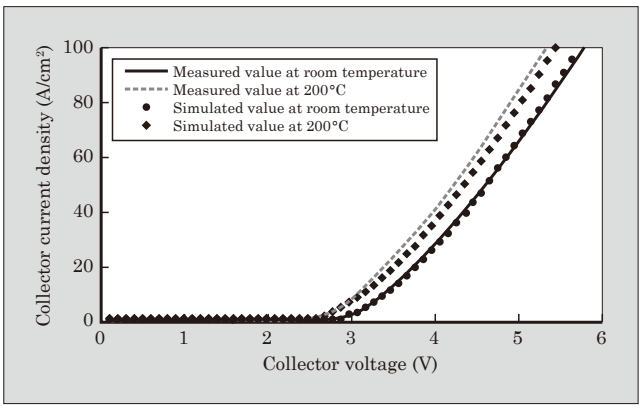

Fig.7 Forward characteristics of 13-kV n-type IGBT

ing voltage than that of the PiN diode is caused by the carrier density on the surface which is still low. We are planning to improve the operating voltage by enhancing the device's surface structure in the future.

3.4 Switching characteristics simulation

Bipolar devices require a longer switching time to draw out carriers injected in high concentration during switching, resulting in a large switching loss. For SiC devices, the thickness of the drift region for keeping the withstand voltage can be reduced to about one-tenth of that of Si devices. Hence, it may be possible to reduce the total amount of the accumulated carriers and cut switching loss. We used a device simulator and a circuit simulator to conduct a switching simulation by taking the inductive load (L load) into account, and predicted the loss in a bipolar device at a bus voltage of 6.6 kV.

The expected switching waveforms of the current structure and the improved structure using the low carrier injection IGBT are shown in Fig. 8. In the current structure, the switching is slow and the transition time is 4 μs or longer. This means that even operation at a carrier frequency of about 1 kHz is difficult. The estimated switching loss is 2 J/pulse or more per active area of 1 cm^2, which can only be used at low carrier frequencies. The cause of the slow switching is the high injection in the IGBT and diode. The following improvements can reduce the switching loss while minimizing the increase of the conduction loss.

(a) Controlling the amount of carrier injection on the back side.
(b) Using a structure to allow the necessary amount of surface carriers to be accumulated.
(c) Dissipating the excessive carriers quickly.

Using a low-injection structure for the IGBT reduces the turn-off switching time to 400 ns, which improves the switching loss. The low-injection PiN diode can also suppress the reverse recovery current and improve the turn-on loss. The loss estimation result with the improved structure is shown in Fig. 9. When compared with a high-injection structure, the switching loss is reduced to 44% and the total loss including the conduction loss at an operating frequency of 2 kHz is improved by 37%.

We compared the characteristics after the improvement with those of Si devices. In order to achieve a 13-kV withstand voltage class device the same as the SiC devices, Si devices are connected in series. Although we should not make a simple comparison, Fig. 10 suggests the probability that a single 13-kV SiC-IGBT has better forward voltage-switching loss trade-off characteristics than those of several Si devices connected in series. When SiC bipolar devices become applicable to ultra-high-withstand voltage applications, a reduction

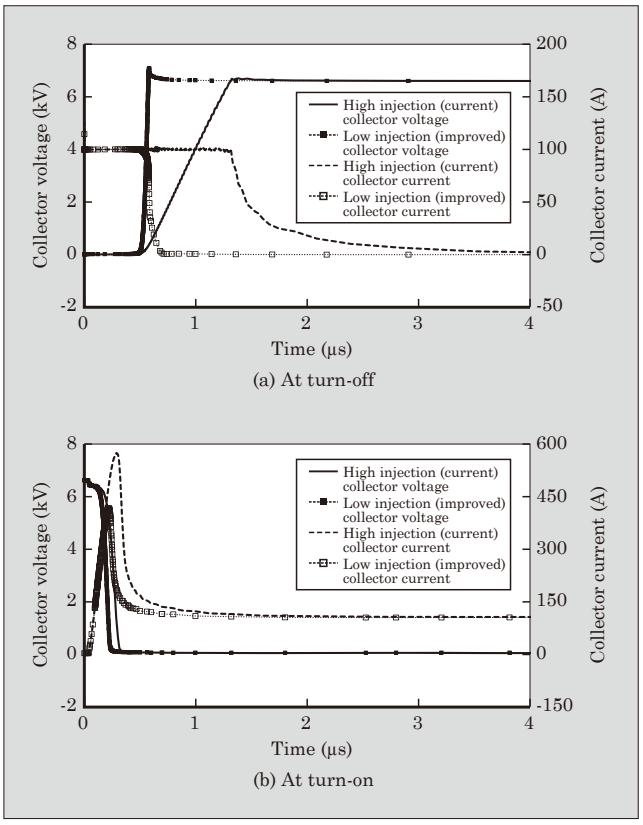

Fig.8 Expected switching waveforms of current structure and improved structure

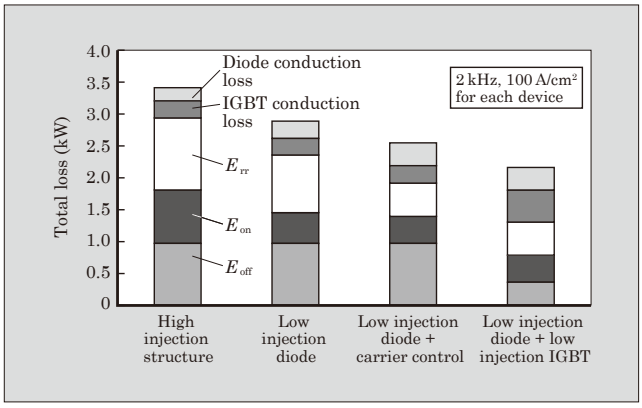

Fig.9 Loss estimation result with the improved structure

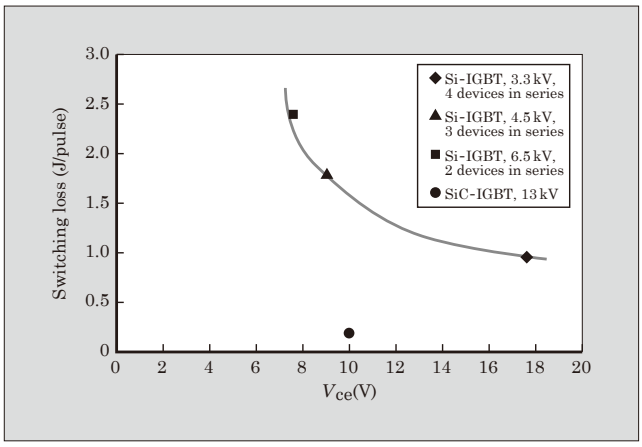

Fig.10 Forward voltage-switching loss trade-off characteristics of devices under 13-kV withstand voltage condition

in loss as well as an improvement of conversion efficiency can be expected.

For example, high-withstand-voltage SiC devices can be used in a reactive power compensator for suppressing the voltage fluctuation in a power system. This enables the current capacity to be reduced and means fewer devices are used, which leads to miniaturization and efficiency improvement of the facility.

4. Postscript

There is a limit to the accuracy of predicting characteristics of ultra-high-withstand voltage bipolar devices because their physical property parameters are lower than those of an ideal crystal. By applying measured physical property values to the simulation parameters and considering the interface charge and parasitic resistance, we could almost reproduce the actual device characteristics. With the progress of process technology, we can expect further improvements in the properties of SiC bipolar devices in the future.

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