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MICREX-F200 SERIES

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1 FOREWORD

MICREX-F200 series (hereinafter abbreviated as F200 series) is enhanced besides in its sequence operating function, adjusting operation, function operation and filing operation, so that the fact makes it an ideal high-speed and high-function programmable controller (hereinafter called PC) that can be applied widely to Process Automation (PA) and Factory Automation (FA).

F200 series is available in two models of processors: FPK200 and FPK205. Their fundamental functions as control computation function have no difference between these two models, but FPK200 is provided with two systems of serial PIO interfaces (T links), while FPK205 has two systems of T link interfaces and high-speed interprocessor interface (P link).

To this series, many new architectures such as function of block diagram language which is a new and simplified version of language EPOL in which we had so much experience with MICREX-E series, as well as direct executing ladder diagram language using exclusive-use LSI's, are adopted. Furthermore, know-hows fed back from our experience with both series of FUJILOG and MICREX-E have been introduced for making this new series easier to use.

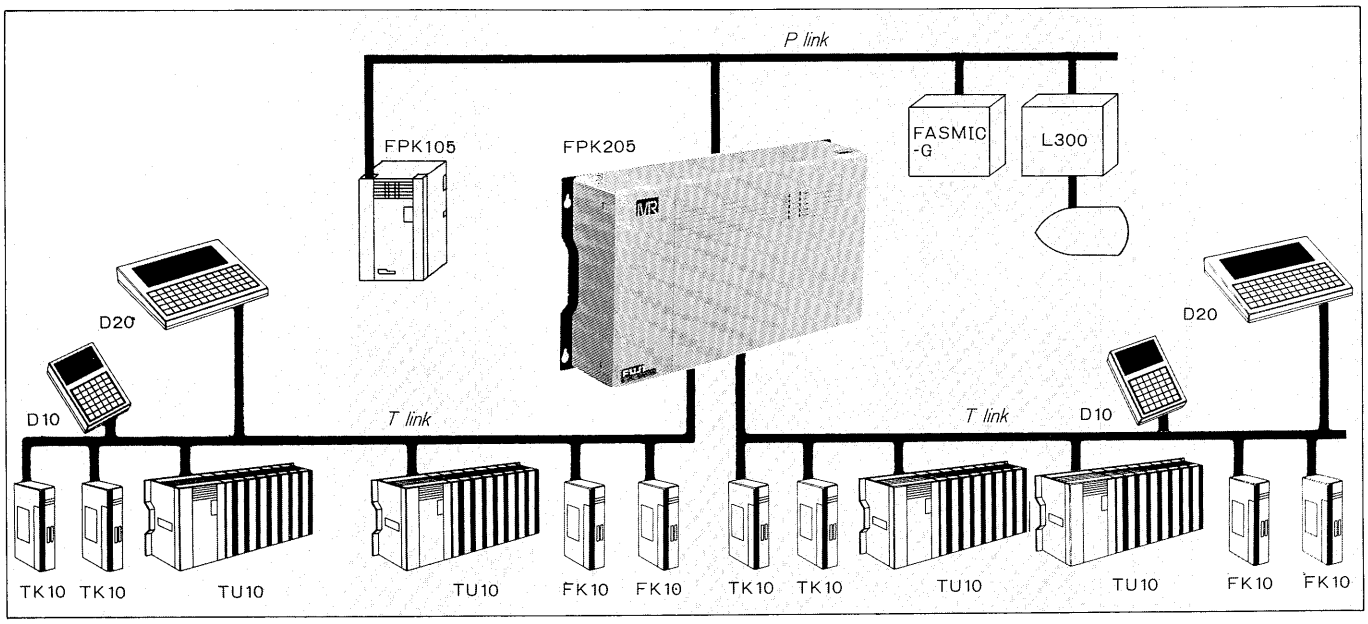
2 FEATURES OF F200 SERIES

FPK200/205 have, besides the features of unified architecture of MICREX-F series (hereinafter abbreviated as F series), the following features:

2.1 High-speed processing

By making the operation processing unit exclusive-use LSI's, the function of processor is made as speedy as that of 0.5 μs for bit computation, and 5~30 μs for numerical value computation, so that this makes this series optimum for controls where there are many numerical value processing. Also, as the standard function is designed to operate BCD 8 digits, no consideration will be required in practice,

Fig. 1 Example of system composition



for carry and overflowing, programming can be made out easily.

2.2 Possibility of executing large-scale controls

Control systems as large scale as 1,024 points (standard) in total of digital inputs/outputs (expansible up to the maximum of 3,200 points) can be architectured.

2.3 Command intensification

In comparison with the MICREX-E series that have been adopted widely for conventional medium-to large-scale control system, data operating instruction (filing instruction) and adjustment operating instruction have been intensified.

2.4 Structuring of software

The notion of function modules (subroutine) that has earned a good reputation as software for MICREX-E series, has been amplified further and improved the linkage function between modules. By this, modularization and hierarchifying of programs are made easier.

2.5 High-speed control response

In addition to cyclic processing, an external interruption processing function that has less overhead is provided, thus making high-speed control response possible.

By simultaneous use of cyclic processing and interruption processing, besides improving the program execution rate, a high-speed control response by process interruption and more elaborate periodical controls through periodical interruption that can be set by multiples of 10 ms are also possible.

Table 1 Specifications of F200 series

Item			Specifications		Remarks
			FPK200	FPK205	
Control system			Stored program system		
Control function			Cyclic operating function		
			Periodical interruption control		10 ms × *n*
			Process interruption control		
Instruction	Language		F-series programming language (FPL)		
	Type		Basic instruction: 19 items Applied instruction: 83 items		
	Operating speed		Sequence operation: 0.5–0.75 μs/instruction Numerical value operation: 5–30 μs/instruction		
	Numerical value operating data system		BCD 8 digits, binary 16/32 bits		
Memory	Data unit	Element	IC-RAM		* denotes memory cassette system, while IC-RAM is provided with battery back-ups.
	Program unit	Element	Standard: IC-RAM Option: EP-ROM*		
		Capacity	28 k steps		
Number of IO points	Digital input/output		1,024 points (expansible up to 3,200 points)		
	Analogue input/output		200 points		
Internal relay data momory	Auxiliary relay/SR		4,096 points		
	Retentive relay/SR		1,024 points		
	Differentiation relay		512 points		
	Step control relay		100 (100 steps)		
	Special relay		560 points		BCB 8 digits
	Timer	0.01 sec.	256 points		
		0.1 sec.	256 points		
	Counter		128 points		BCB 8 digits
	Word memory		4k word		1 word = 32 bits
	File memory		4k word		1 word = 16 bits
	P link relay		–	8,192 points	
	P-link memory	High speed	–	2 k words	Including P-link relay
		Low speed	–	6 k words	
T link	No. of links		2		Remote PIO
	No. of capsules connected		32 × 2		
P link	No. of links		–	1	
Type of input/output			According to F series standard input/output interface		
General specifications			According to F series basic specifications		
Body outer dimensions (mm)			450 (W) × 250 (H) × 100 (D)		Mountable to 19-inch rack

3 SYSTEM COMPOSITION AND SPECIFICATIONS

3.1 System composition

An example of system compositions of F200 series is shown in *Fig. 1*. Two types of processors are available for this series, namely, FPK200 and FPK205. Both are provided with two systems of terminal network (T links) interfaces, through which they can be coupled with various PIO's and program loaders. Further, FPK205 is provided with processor network (P link) coupling function and can be used as an interface with other controllers.

3.2 Specifications

Table 1 shows specifications of F200 series.

4 CONTROL SYSTEM AND OPERATION

4.1 Control system

FPK200/205 are controlled by microprogram (firmware). Numerical instruction and filing instruction are executed by word processor directly connected to the microprogram. Also, the bit processor that executes directly the ladder diagram, transmission LSI interfacing with T link, and P link processor interfacing with P link operate under the control of the microprogram.

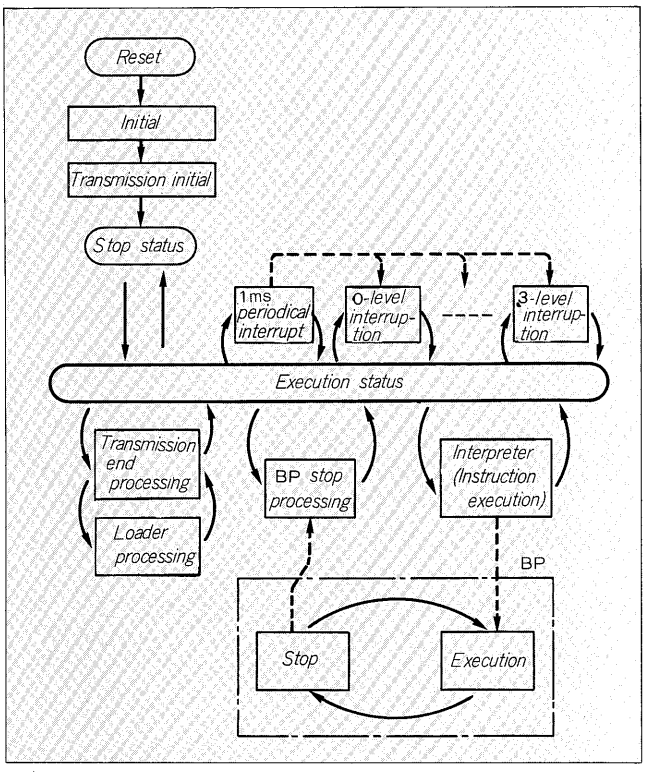
Fig. 2 shows the processing flow of the firmware and in the following, the outline of the control function is described.

4.1.1 Initial processing

The initial processing is started by start command and processes the following:

(1) Starting of micro-diagnosis
(2) Read-in of memory cassette
(3) Making up of control table
(4) Initial set for various register

Fig. 2 Firmware processing flow



4.1.2 Execution of application program

When the application program is executed, the bit processor will process the ladder diagram as it is in a form of picture. When the bit processor detects the word processing instruction, processing will be transferred to the word processor. While the bit processor is processing the program, the word processor executes starting of transmission LSI, periodical timer processing and RAS processing. The program where there are jointly sequence process and numerical process as this, by using opportunely both bit and word processors, will be efficiently processed.

4.1.3 Input/output data processing

The input/output data regions are 1:1 assigned according to the prefix number of PIO capsule. The data transmission between F200 and PIO capsules are carried out with read-out and write-in for this region.

Input data from PIO capsule are refreshed in periodical cycle, and the output data to PIO capsule are carried out in synchronization with CHT (Check and Transfer) command written in the application program. And when there is no CHT command, it's performed at the scanning end of the program.

4.1.4 Data management

Operation data are managed arranged by each data form. The standard data form is that of BCD 8 digits, however another form, binary integer form is also available. Operations among data of different forms are executed internally in an automatic form, in the application program, there is no need to consider the conversion but only to designate the data form.

4.1.5 Micro-diagnosis

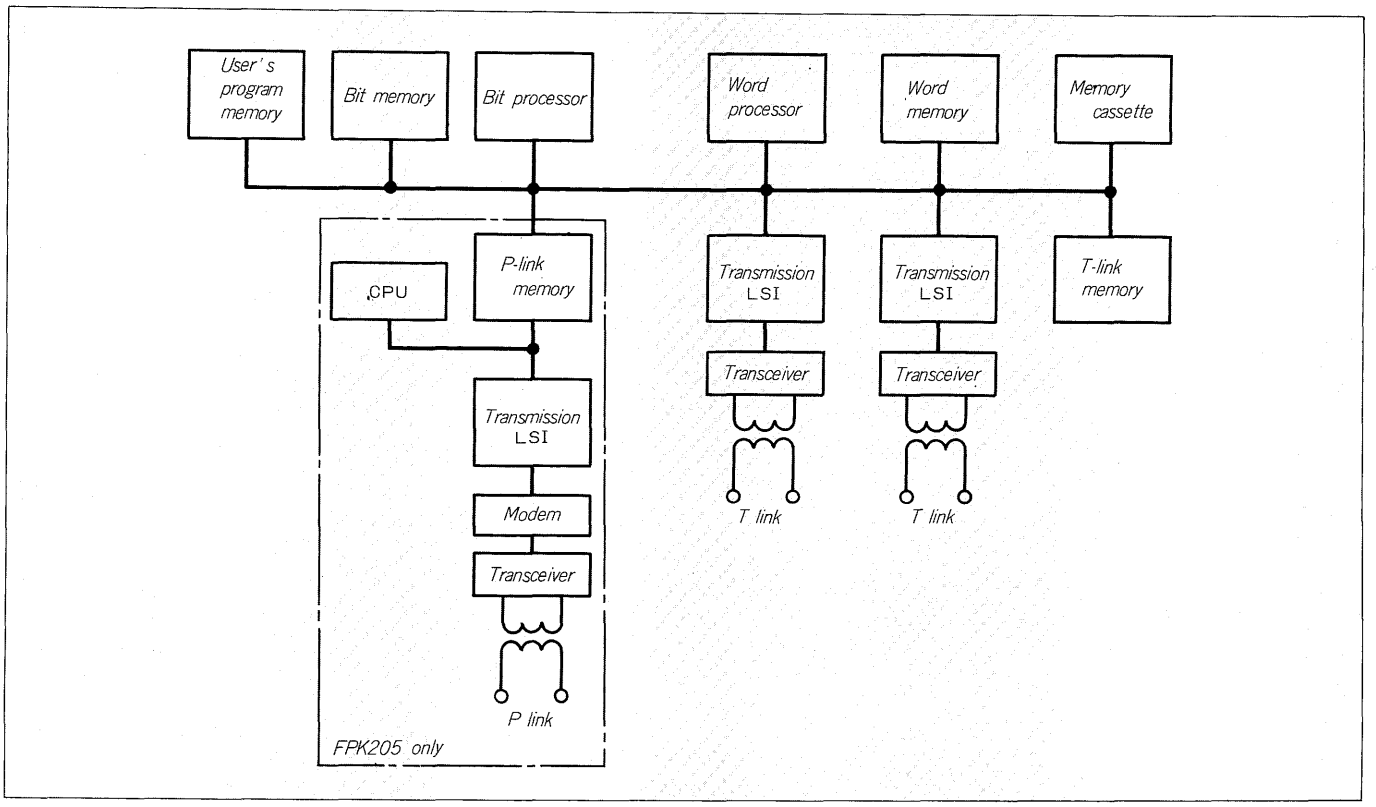
Fundamental hardware diagnosis such as word processor operating function and register read/write is carried out by micro-program.

The micro-diagnosis is started at the time of initial and at the time of executing the CHT instruction. At the time of initial, all check items will be diagnosed and at the time of CHT instruction execution, only important items will be diagnosed.

4.2 Manipulation

All operations of FPK200/205 such as system start/stop, change-over of operating modes are carried out from the front control panel. There are two starting methods, namely, AUTO mode and MANUAL mode. In AUTO mode, when the power is thrown in, the machine will enter in operating status automatically, while in MANUAL mode, after throwing in the power, by depressing the start switch, the machine will enter in operating status. Also, there are two modes in operation modes, that is, RUN mode that carries out the normal operation and another, TEST mode. When set to TEST mode, PIO output will be retained as it

Fig. 3 Hardware block diagram



is even when the processor has come to a stop.

5 HARDWARE

5.1 Composition

Block diagram of the hardware is shown in *Fig. 3*.

The hardware of this system is composed of word processor for processing word operation, bit processor for bit operation processing, T link interface, P-link interface and each memory, having the following features.

(1) Compact hardware

By adopting LSI of exclusive use and hybrid IC's, hardware is simplified and high-function is attained with a compact size.

(2) High-speed processing

Thanks to development of exclusive-use LSI's and adoption of microprogram control system, high speeding of word operation processing and bit operation processing is attained and, at the same time, by divided processing on the processor level, high speed processing as a whole could have been obtained.

(3) T link interface

By large-scale integrated T-link interface, high speed and long-distance transmission of PIO data are obtained. With this configuration, PIO dispersion type system with total I/O's of 1,024 points can be constructed.

(4) P-link interface

FPK205 has a P link interface function and can transmit high-speed data between processor and capsule 5M bits/sec.).

(5) Low power consumption

Thanks to making the circuit components LSI's of exclusive use and CMOS, power consumption of the equipment is much reduced. The cooling system is that by natural air.

5.2 Exclusive-use LSI

By adopting LSI of exclusive use for hardware consti-

Fig. 4 Program composition

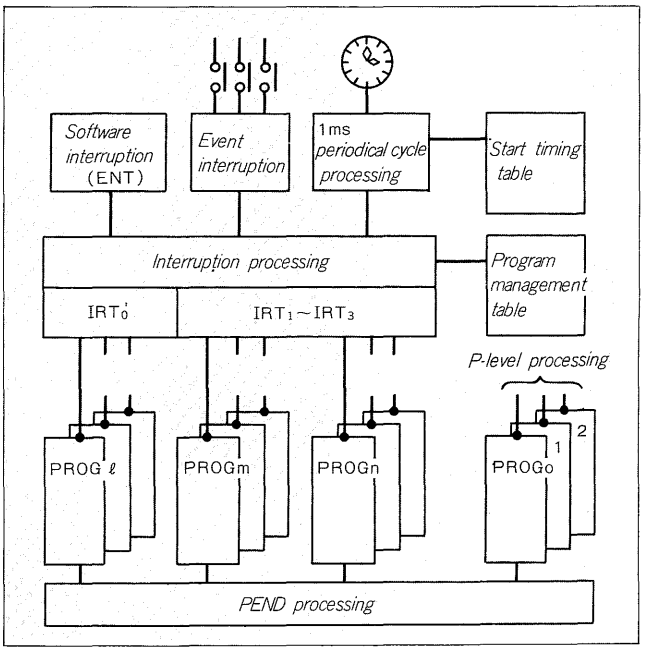


Table 2 List of commands

Classification	Designation	Symbol
Sequence	a contact	—||—
	b contact	—|/|—
	Coil	—( )—
	Set	—(S)—
	Reset	—(R)—
	Rising edge differential	—(↑)—
	Falling edge differential	—(↓)—
	Inverse	—/—
	Shift register	SR
Timer	Step sequence	Sxx.xx Sxx.xx —||— ( )—
	ON delay timer	TON
	OFF delay timer	TOF
	Integrating timer	S TMR R
	Mono stable	MS
	Mono stable (Retriggerable)	MR
Counter	Counter	↑ CTR R
	Down counter	↓ CTD R
	Updown counter	↑ UDCT ↓ R
	Ring counter	↑ RCTR R

Classification	Designation	Symbol
Arithmetical Operation	Addition	+
	Subtraction	−
	Multiplication	×
	Division	÷
	Rounding	÷R
	Root	√
	Absolute value	ABS
	Change sign	+/−
	Increment	+1
	Decrement	−1
Comparison	>	>
	≧	>=
	=	=
	≦	<=
	<	<
	≠	≠
	File comparison	REF
Logic Operation	AND	AND
	OR	OR
	EOR	EOR
	Inversion	INV
	SHIFT right logical	SRL
	Shift left logical	SLL
	Set bit	SBIT
	Reset bit	RBIT
	Test bit	TBIT
Conversion	Binary/BCD	BCD
	BCD/Binary	BIN
	Decode	DECO
	Encode	ENCO
	7 Segment	7SEG
	Count ON-bit	BCNT
Arithmetic Function	sin	SIN
	cos	COS
	tan	TAN
	$\sin^{-1}$	ASIN
	$\cos^{-1}$	ACOS
	$\tan^{-1}$	ATAN

Classification	Designation	Symbol
Transfer	Move	MOV
	Block move	BT
	Move digit	DT
	Move upper digit	MOVU
	Move lower digit	MOVL
	Pattern clear	PC
	Search	SRCH
	Switch	SW
Analog	Upper limit	
	Lower limit	
	Upper/lower limit	
	Dead zone	
	Bias	
	Filter	FIL
	Differential	DIF
	Integration	INT
	Sample hold	HOLD
	Multi percent	MLTP
	Divide percent	DIVP
File	Store FIFO (FILO)	FFST
	Load FIFO	FIFO
	Load FILO	FILO
	Define file	FILE
	Clear file	FLCL
	Selector	SEL
	Deselector	DSEL
	File read-out	RFIL
	File write-in	WFIL
	File information	FINF
Program control	Program entry	PROG
	Program end	PEND
	FM call	FM
	FM start	FMS
	FM end	FME
Branch	Skip	SKIP
	Skip end	SEND
	Negative skip	NSKP
	Jump	JMP
	Jump end	JEND
Loop	Loop	LOOP
	Continue	CONT
System	PUSH	PUSH
	POP	POP
	LEA	LEA
	CHT	CHT

tuting a core of internal control of this system, improvement in processing speed and perfectioning of function are deviced. In the following, the outline of each LSI is described.

(1) Word processor

This is a bit slice type high-speed processor, and effectuates controls on circuits associated with numerical operation processing.

For numerical operation, multiplication and division can easily be done and as it is provided with BCD correcting function, it can process the block diagram language with high speed.

(2) Bit processor

This is the LSI executing directly the ladder diagram language in picture form as it is. In this system, an average processing speed of 0.5 μs/point is attained by making memory access of the bit processor high speed.

(3) T link: P link interface

T link interface is composed of transmission LSI of exclusive use and hybrid IC for line interface. The transmission LSI executes DMA for T-link memory, parrallel/serial conversion of transmission data and modulation/demodulation. Hybrid IC is a transceiver for transmission line.

P link interface is composed of the same transmission LSI as that of T-link interface, hybrid IC and high-speed modem LSI.

6 SOFTWARE

6.1 Program composition

Fig. 4 shows the program composition. Programs are available in two types, namely, one is P-level program constantly started in a cyclic form and interruption program composed, in its turn, of 4-stage levels. P level program can be registered up to 16, and interruption program, up to 8 per each level (in total of 32).

The interruption program is used in case when a high-speed control response and precise cycle control are required. 0-level interruption program is given the highest priority level, and as for the interruption factors, there are power source failure, T link failure and P link failure. 1-level interruption program is started all by the event interruption from the processing side. The 2- and 3-level programs are provided as periodical interruption program, and since the interruption cycle can be freely set by application, it can be applied efficiently in the field where minute control cycles are required.

6.2 Programming language

A list of programming language that can be used in F200 series is shown in *Table 2*.

The program language of this series has the following features:

(1) It has a compatibility for higher hierarchy with F100 series.

(2) It has a wide-range of programming language as a general-purpose controller and can process data and execute filing operation..

(3) With it, it is easy to make programs modules and hierarchies, and it can register also the program as a standard module.

7 CONCLUSION

PA and FA in the recent industrial sectors demand more and more high speed and high function for PC's. F200 series is a high function distributed type PC developed in reply to such needs, and it is provided with a variety of instruction set suitable for PA and FA, and it has realized high-function distributed control through adoption of F-Net common to F series.

This article describes the outline of composition, specificaiton, hardware and software of F200 series.

From now on, we intend to expand the field of application of F200 series, improve the ease of its use, and propel the perfectioning of peripheral devices and supporting equipment, together with development of equipment of superior hierarchy so that this F200 series would be that of equipment of easy access to every user.