PROGRAMMING LOADER "UT33A" "UT34A" "UT35P"

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I. INTRODUCTION

For Fuji general purpose programmable controllers (hereinafter abbreviated to as PC) FUJILOG- μ B, - μ T and - μ H, various programming equipment have been prepared so that program loading, test operation, maintenance, inspection and documentation can be made easily.

The main functions that programming equipment must have are:

- (1) Reading, writing, changing and correcting programs.
- (2) Monitoring function (signal status display)
- (3) Keeping and reproducing programs.
- (4) Hard copy

For Fuji general purpose PC, the following programming equipment are available,

- (1) Samll size loader which can be operated and carried easily as of its small dimensions and light weight.
- (2) High function type loader which combines various equipment.
- (3) Loader with PROM writer for PCs used strictly for PROM.
- (4) CRT loader with which reading and writing can be done in the form of a ladder.

This paper explains the small size loader and high function type loader out of (1) through (4) above.

II. SYSTEM CONFIGURATION

Out of the programming loaders connected to PC FUJILOG Series, the portable type is classified into the small size loader and high function type loader, and further, depending on the objective PC, they are classified into those for JUJILOG- μ T, μ B and μ H.

1. Small size loader UT33A for FUJILOG- μ T and - μ B

Based on an 8 bit micro-processor, this loader consists of a memory, 7-segment LED, 6×5 keyboard, and parallel communication interface used to connect the loader with the PC proper. Because of its biggest feature "Small dimensions" the printed circuit board is compactly arranged, power is supplied from the PC proper and thus, the

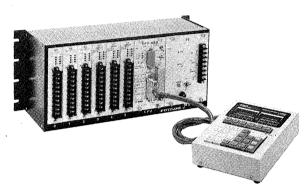


Fig. 1 Appearance of programming loader UT33A

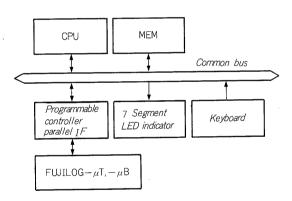


Fig. 2 System configuration of UT33A

loader dimensions are equivalent to those of an ordinary electronic calculator. *Fig. 1* and 2 shown the appearance and system configuration respectively.

2. High function type loader UT35P for FUJILOG- μ T and $-\mu$ B

This loader has digital cassette MT, EPROM writer and printer in addition to the components of the above introduced loader UT33A. Also added is a function to transfer program contents among each equipment, enhancing the program maintenanceability. For the indicator, 16×2 character liquid crystal display is used, realizing readily watched instructions and precise message display. This



Fig. 3 Appearance of programming loader UT35P

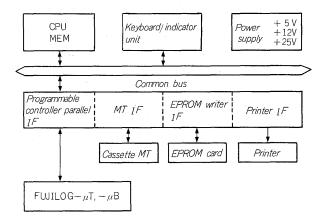


Fig. 4 System configuration of UT35P



Fig. 5 Appearance of programming loader UT34A

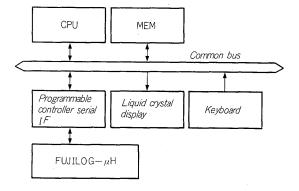


Fig. 6 System configuration of UT34A

loader is accommodated in a compact portable case so that the loader can be carried conveniently. Fig. 3 shows the appearance, and Fig. 4 shows the system configuration.

3. Small size loader UT34A for FUJILOG-μH

Based on UT33A, keys are added to this loader so that the instructions added by FUJILOG- μ H can be programmed. For the indicator, 16×2 character liquid crystal display is used, and for high speed monitoring, LED is also used. This loader is connected to the PC proper through a serial communication interface.

Figs. 5 and 6 shows the appearance and system configuration respectively.

III. SPECIFICATIONS AND FUNCTIONS

1. Specifications

Table 1 shows the specifications of each portable type programming loader.

2. Functions

Table 2 shows the programming function of each loader. When developing a controller with a PC used, out of those functional items indicated in the Table 2, the programming and monitoring are required at least. In addition to these functions, to ease debugging, simulation function is also employed. Further, for the high function type loader, program keeping function and loading function are added.

1) Programming

The programs executed by the associated PC are witten by each step and inserted or deleted in multiple steps by using symbolically indicated keys (R, A, O, W, etc.) and number keys. Combinations which are not established as an instruction and setting outside the address range are notified to the operator by the indicator or buzzer. The retrieval function can be made either to the positive (+) direction (program step increasing direction) or negative (-) direction (program step reducing direction). For example, when changing an input/output address to other address, at which step the access is being made to that address can be found by a single operation. For UT34A, sequence expanding instructions are added to FUJILOG-μH, and as programming is made by EM number, the EM number can be indicated in a mnemonic system as shown in the Table 3.

2) Monitor

For test operations of a controller, debugging is required to eliminate errors on the programs written in the PC and input/output connection errors. The monitoring functions of this loader allow input/output signals, ON-OFF status of the data memory, present values of the timer and counter and results of arithmetic operations during program execution (ARG memory) being indicated without stopping PC operations. In case of UT35P, any desired eight points can be selected, and these points can be simultaneously monitored. This function is effective when

Table 1 Specifications of UT33A, UT34A and UT35P

Unit type				UT33A	UT35P	UT34A		
	Objective programmable controller			FUJILO	FUJILOG-μH			
Application		Program memory		204	8192 steps			
	Objective processing range	Data memory	<u> </u>	12	1024 cards			
		Number of I/O)	250	512 points			
		Processing instr	ruction	FUJILOG-μT and	FUJILOG-μH all instructions			
	Internal control system			8 bit micro-computer system				
suc	Power failure backup memory			_	used	_		
Control specifications	Auxiliary device			-	Digital cassette MT, EPROM writer and printer	-		
spec	Input system			Key input by symbolic language				
ntrol	Display system			7 segment LED + LED	16 x 2 character liquid co	crystal display + LED		
Co	Communication system with programmable controller			Pa	Serial			
sue	Power supply			Receives from PC proper	Maximum	Receives from PC proper		
General specifications	Ambient conditions for use			0~45°C 10~85%RH without condensation	5~40°C 20~80%RH without condensation	0~45°C 10~85%RH without condensation		
	Cooling system			Self-cooling	Forced cooling	Self-cooling		
	Approx. dimensions (mm)		210 × 150 × 63	450 × 330 × 150	230 × 140 × 60			
Ger	Weight (kg)		1.2	12	1.1			

Table 2 Functions of UT33A, UT34A and UT35P

Item	Unit type	UT33A	UT35P	UT34A	·
Programming	Writing Reading Inserting/deleting Changing/correcting All erase Device/undefined instruction retrieval Data memory backup area setting	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0	Can be operated when CPU stops (program mode). However, program read and retrieval can be made even during operation (run mode).
Monitor	Monitoring ARG memory Monitoring I/O card signal Monitoring data memory Monitoring timer counter valve Simultaneously monitoring any desired eight points	0 0 0 -	0 0 0	0 0 0	1 or 8 bit selection can be made. For UT34A, eight bits can be indicated in decimal. Decimal indication of the present value
no on	Forced ON-OFF of input/output	0	0	0	Possible regardless of CPU operation or stop
Simu- lation	Calculating cycle time	_	_	0	For FUJILOG-μT and -μB, cycle time is fixed at 20 mscc.
	Copying program by digital cassette MT.	-	0	<u>-</u>	Program contents can be copied mutually among PC proper, loader and cassette MT.
Program keeping	Writing into EPROM	_	0	_	Program contents of PC proper, loader and cassette MT can be written into EPROM.
ogram]	Copying by printer	_	0		Program contents of PC proper, loader and cassette MT can be copied on the printer
Pr	verifying	_	0	_	Program contents can be verified mutually among PC, loader, cassette MT and EPROM.
Operating error detection		0	0	0	Key operation error, undefined instruction, overflow of number of program steps and card address are alarmed by display or buzzer.
Equipment operation error detection		0	0	0	Improper connection with PC proper, program control error during operation, memory write error and CPU operation error are detected and indicated.

Table 3 Expanded instruction display of UT34A

	Instructio ral expres		Instruction (mnemonic expression)	
EM	0/	1000	LD	1000
EM	2/	1010	ST	1010
EM	10/	1020	ADD	1020
EM	14/	1021	SUB	1021
EM	18/	900	СР	900
EM	24		INV	- "
EM	26		INC	
EM	28		SRC	

checking mutual operating timings of contacts.

3) Simulation

When debugging programs, status of each signal is checked by giving dummy input signals. In this case, ON-OFF signals can be given forcedly from the programming loader without turning inputs of the PC on and off actually.

4) Keeping programs

UT 35P is equipped with cassette MT, EPROM writer and printer, and therefore, programs can be kept and verified.

For the cassette MT, a digital cassette MT is employed to improve reliability and transfer speed, and writing can be done from the PC to the cassette within about 10 seconds.

The EPROM writer is used to write programs into the EPROM. The initial program preparation is executed by using RAM card, and after confirming the programs through debugging and test operations, the programs are written finally by this EPROM writer. When erasing the programs, EPROM eraser UT3201P (See Fig. 7) prepared for this system is available.

Using the printer, contents of the program memory within the PC, cassette MT and PROM card can be printed out. Written programs can be checked with the program sheet easily, and by the automatic preparation of the final program list, documents can be prepared easily. Fig. 8 shows the printing format.

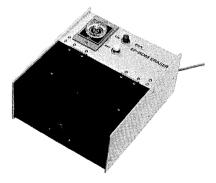


Fig. 7 EPROM eraser UT3201P

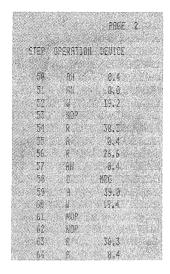


Fig. 8 Program list example of UT35P

IV. PROGRAMMING

A controller desing using a PC is similar to that of ordinary relay sequence controller, Fig. 9 is a flow chart which indicates a controller system design using a PC.

1) System design

The control system is decided based on the system specifications of the controller, scale of the applicable

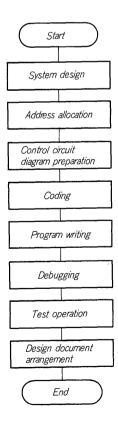


Fig. 9 Procedure flow chart for control system design

PC, types of input/output cards (AC/DC, voltage, contact/contactless), number of input/output points, etc. are decided next.

2) Address allocations

Destinations of lines connected to the I/O unit of the PC and signal grouping are taken into consideration, and addresses are allocated to input/output signals. At the same

time, for the timer, counter and auxiliary relays, allocations are made within the internal data memory, and all the signal addresses are decided to designate backup area in the data memory for power failure.

3) Preparating control circuit

Since programmings of the PC are performed in accordance with the control circuit, a control circuit

Operated item		Run mode		Output control	Operation procedure			
operated item		Run	Stop	switch		Remarks		
	Program writing	No	Yes	Either ON or OFF	(Calling out any desired step) \rightarrow (Instruction set) \rightarrow ENT			
Programming	Program insertion	No	Yes	, , , , , , , , , , , , , , , , , , , ,	 (1) Insertion of one instruction (Calling out inserted step) → (Instruction set) → INST (2) Insertion of successive multiple instruction (circuit block) (Calling out inserted head step) → (Setting number of inserted instructions) → INST (Writing one instruction by one instruction) 	Insertion of multiple number of NOPs		
	Program deletion	Νο	Yes	n	(1) Deletion of one instruction (Calling out deleted step) → □ELT (2) Deletion of successive multiple instruction (circuit block) (Calling out deleted head step) → (Setting number of deleted instructions) → □ELT			
	Desired card and relay retrieval	Yes	Yes	п	(Calling out retrieved head step) \rightarrow (Setting retrieved card or relay address) Retrieved from called out step $+1$ step up to 8191 steps toward the step increasing direction Retrieved from called out step -1 step down to 0 step toward the step reducing direction (When retrieving successively, push the instruction key indicated at that step to erase the instruction code portion, and again push $+$ SRCH or $+$ Retrieved from called out step -1 step down to 0 step toward the step instruction code portion,			
	Back up area setting	No	Yes	711	$ \begin{array}{c} $			
Simulation	Data memory monitoring	Yes	Yes	n .	 (1) Reading out contact unit C → CARD → (Setting bit address) → CALL (2) Reading out card unit C → CARD → (Setting card address) → CALL 	Indicated in ARG display Indicated on eight LEDs		
	Timer counter present value monitoring	Yes	Yes	"	$(Note)$ $C \rightarrow CARD \rightarrow CTR \text{ or } CTR TMR OTR OTR \text$	Remained value indication Up signal is indicated on ARG display		
	I/O control	Yes	Yes	LED	(Reading out controlled relay) → Corresponding relay ON OFF: Corresponding relay OFF			
	Execution speed check	Yes	Yes	. ,,	$ \begin{array}{c} (Note) \\ \hline CHK \\ \vdots \\ \rightarrow \end{array} \rightarrow \begin{array}{c} 2 \end{array} \rightarrow \begin{array}{c} G0 \end{array} $			

Fig. 10 Key operation procedure of programming loader

diagram must be prepared. For the control circuit diagram, a contact relay sequence is suited, and it does not differ from an ordinary relay circuit. Depending on a PC, however, it may perform processings in the unit of byte, and it should be noted that the circuit diagram may not be expressed with ordinary relay symbols only. Further, it will be convenient to segregate the contact circuits within the PC from the external contact circuits on the circuit diagram.

4) Coding

Based on the prepared address sheet and control circuit diagram, a list expressed in a mnemonic system is prepared by using each instruction. This is the control program. A special program sheet is available so that the program memory can be kept and wiring can be made onto the program memory conveniently.

5) Writing programs.

Programs are written by operating keys with the programming loader connected to the PC in accordance with the contents of the program sheet prepared as described in 4) above.

6) Debugging

In some cases, the programs written in the PC may contain a sequence error or writing error due to an erroneous key operation. This debugging is equivalent to the sequence check in a relay sequence. Output signal status is checked by giving a dummy input signal, and signal status of internal data memory is checked by using monitoring functions of the programming loader. If any errors are detected, corrections are made by using the programming loader.

7) Test operation

Test operations are made by connecting the programming loader to the machine or equipment to be controlled, and by collating with the system specifications, the actual control contents are checked. During the test operations, differences between the circuit design and control contents,

deviations in timing, etc. which could not be expected when designing the system may appear, and these differences and deviations must be changed or corrected quickly. As a function of the programming loader, it is important, in addition to the ordinary program preparations, that the corrective operations can be done quickly and correctly at the site.

8) Arranging design documents

For the programs completed by repeating the corrections and changes as described above, the control circuit diagram should be followed up and the programs should be printed out on a hard copy immediately so that with which programs the system is being presently operated can be made clear when an addition or change of the specifications of the system itself occurs. For this purpose, the high function type loader is capable of obtaining digital cassette MT and hard copy by using the printer. Further, with the EPROM wirter, PROM of programs can also be made.

V. PROGRAMMING LOADER OPERATING EXAMPLE

The programming method of UT33A PC is exactly same as that of UT35P. UT34A PC follows the operations of the UT33A, and is capable of programming instructions added by FUJILOG- μ H also. Fig. 10 shows programming loader key operating procedure.

VI. POST SCRIPT

Both the small size loaders and high function loader perform programmings with sequence control instruction words such as R, A, O, and W, and because of their simply operated features, the demands are increasing. We hope the users will fully utilize these loaders to reduce delivery time of sequence controller panels.