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CMOS PROCESS TECHNOLOGY

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1. FOREWORD

The high performance and high grade of electronic equipment and systems is accompanied by a steady strengthening of the demand for high integration and high performance of even the integrated circuit which are important elements in realizing these.

There is also an amazing growth of micro photolithography for the movement toward expansion of system functions and CMOSIC technology, with such features as low power consumption, fast operation, high density integration, etc., is becoming the mainstream.

Against such a background, Fuji Electric is pouring much power into CMOS process technology. As a result, high quality custom IC products, together with technology featuring high voltage, built in sensor, and bump based mounting technology, are offered to the market.

The features of Fuji Electric CMOS process technology and examples of its application to IC are outlined.

2. Si-GATE CMOS PROCESS

The Si-gate CMOS process has special features of Si-gate technology, such as:

(1) Micro photolithography which allows formation of the gate and source, drain region by self-align is possible.
(2) Speeding up is possible because of reduction of the gate and source, drain overlap capacity.
(3) A low threshold voltage device is obtained easily because of work function difference between gate electrode and substrate.
(4) High degree of interconnection design freedom which allows use of polysilicon interconnection.
(5) Since it is covered with polysilicon immediately after gate oxidation, the possibility of contamination is small.

In addition, CMOS construction as the origin, low power consumption, and a high noise margin are featured.

Fuji Electric has the Si-gate CMOS processes shown in *Table 1* and can deal with numerous customized applications.

The 6 μm and 2 μm CMOS process technologies are described below as typical examples of these Si-gate CMOS process technologies.

Table 1 CMOS process technology table

Process technology	Design rule (μm)	Poly-silicon	Metal	Power supply voltage (V)	Maximum clock frequency (MHz)
Si-gate CMOS	6	1 layer	1 layer	30	8
	4	1 layer	1 layer	14	15
	2	1 layer	1 layer/2 layers	7	20
	1.5	2 layers	1 layer	7	30

3. 6 μm CMOS PROCESS TECHNOLOGY

3.1 Process

A feature of the 6 μm CMOS process is that a high voltage is possible. Moreover,

(1) A 5 V logic system and high voltage (30 V) output stage can be realized by the same process.
(2) The process can be simplified and a low threshold voltage device can be formed by the two conductive type polysilicon gate process.
(3) High resistivity polysilicon formation is easy.

etc., are also featured.

3.2 Device characteristics

The high voltage Nch FET and Pch FET voltage-current characteristics at the 6 μm CMOS process are shown in *Fig. 1* and *Fig. 2*. The voltage range is shown up to the absolute maximum rating 30 V, but an actual avalanche breakdown voltage over 37 V is secured.

Next, the device characteristics of the low voltage logic section are shown in *Fig. 3* and *Fig. 4*. Both show I_D-V_D characteristics when the gate voltage is changed in 5 V steps.

3.3 Application exmaples

A chip photograph of the FD3805F common driver suitable for driving a large size dot matrix LCD panel is shown in *Fig. 5*. This device featires 80 output, 28 V driven voltage, 1/64~1/240 signal pulse duty, and date shift direction switching and can be applied to a wide range of LCD

Fig. 1 High voltage n channel FET voltage-current characteristics

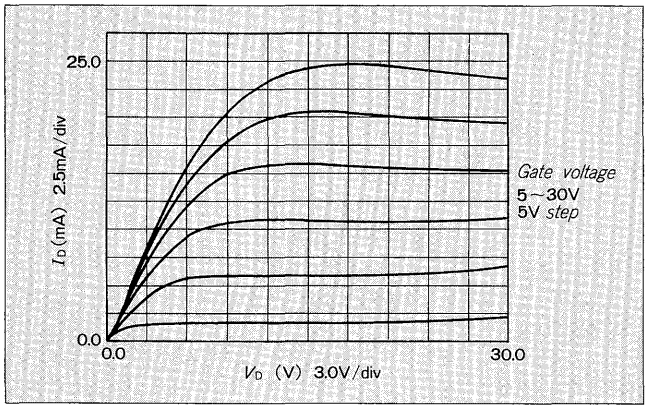


Fig. 2 High voltage p channel FET voltage-current characteristics

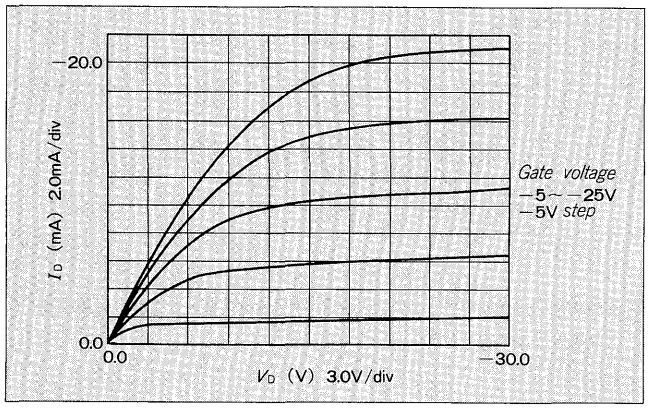


Fig. 3 Logic section n channel FET voltage-current characteristics

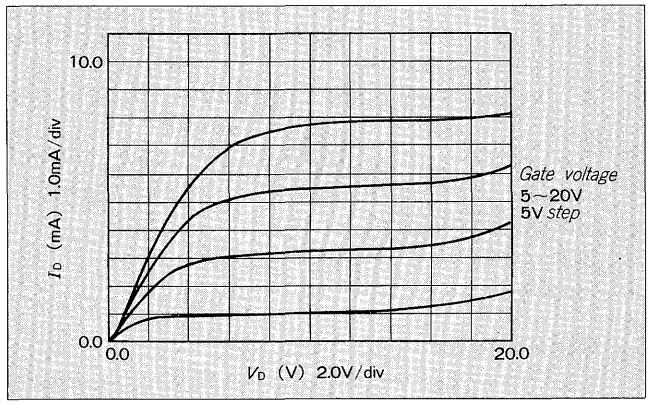


Fig. 4 Logic section p channel FET voltage-current characteristics

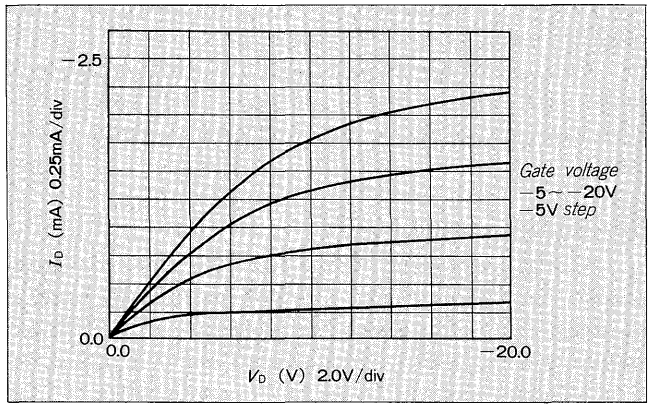


Fig. 5 IC for general purpose LCD panel drive

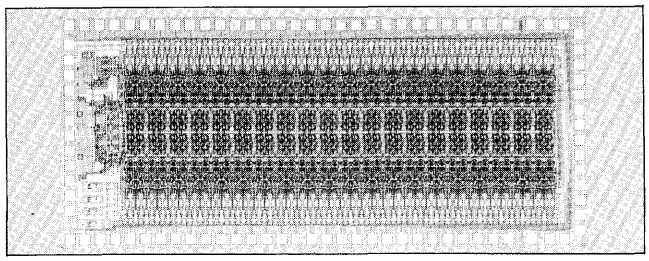


Table 2 Absolute maximum ratings of common driver IC

Item	Symbol	Rating	Units	Remarks
Power supply voltage	V_{SS}	−7~0.3	V	
Driven voltage	$V_{0,\,1,\,4}$	−30~0.3	V	Note 1
Driven voltage	V_{EE}	−30~0.3	V	Note 2
Logic input voltage	V_I	V_{SS}−0.3~0.3	V	
Operating junction temperature range	T_j	125	°C	
Storage temperature	T_{ST}	−40~150	°C	

Note 1: $V_{0,\,1,\,4}$ shall satisfy $V_{DD} \geqq V_0 > V_1 > V_4$.
Note 2: Voltage values are all based on V_{DD}=0.

Fig. 6 2 μm CMOS process flow and cross-section construction

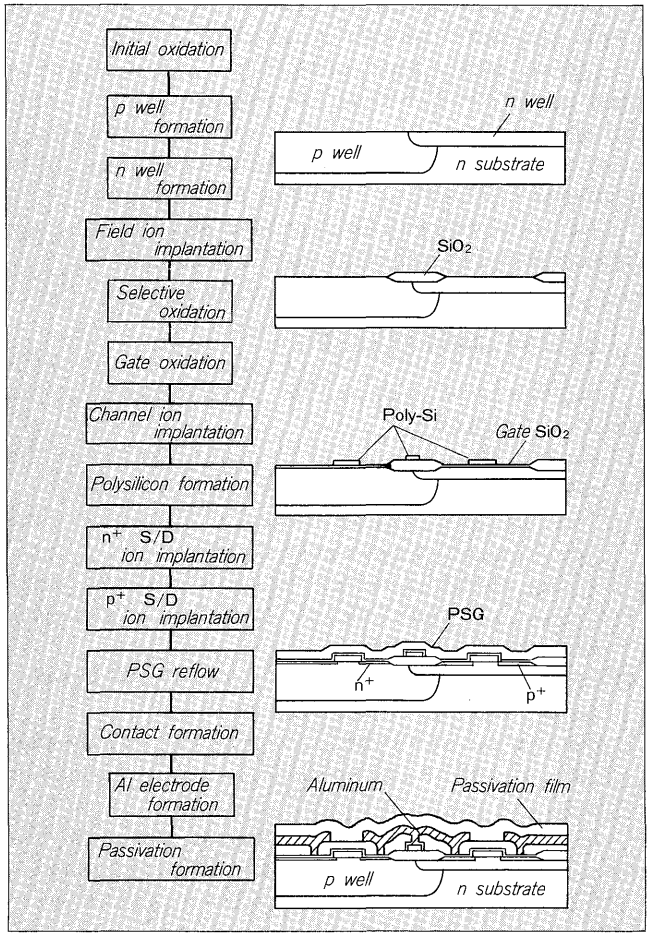


Fig. 7 Aluminum electrode pattern example

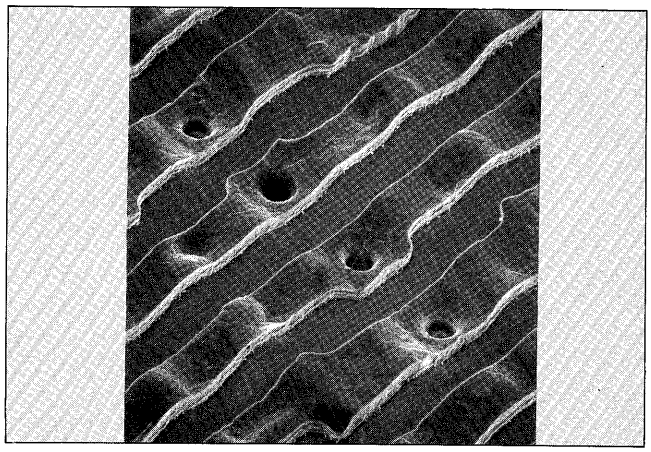
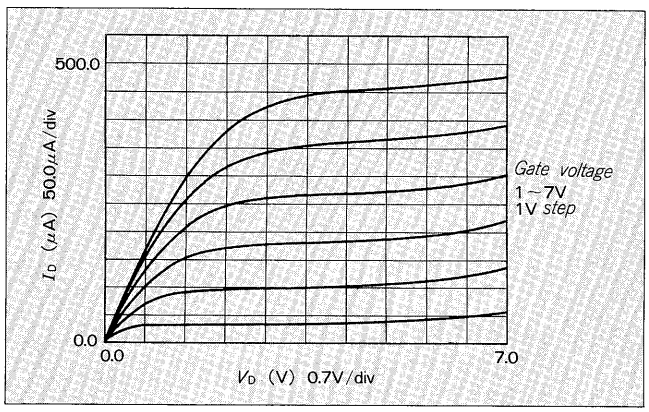


Fig. 8 2 μm CMOS n channel FET voltage-current characteristics



panels by combining it with the FD3806F segment driver developed as a pair. Its absolute maximum ratings are shown in *Table 2.*

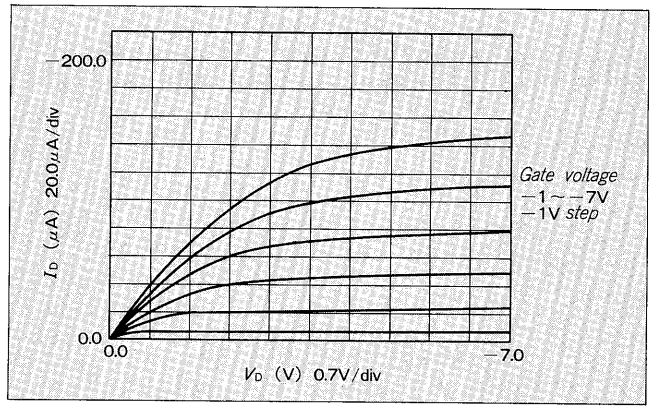
4. 2 μm CMOS PROCESS TECHNOLOGY

4.1 Process

Basically, the 2 μm CMOS process was developed with possibility of direct application to 1.5 μm CMOS technology. Its main features are:

(1) Pwell/Nwell twin well

Fig. 9 2 μm CMOS p channel FET voltage-current characteristics



(2) Minimization (8) of the photomasking steps and other rationalization processes

(3) Threshold voltage control is easy.

(4) Excellent surface planarization

(5) Photosensor, etc. can be built in.

The example of aluminum electrode pattern formation on PSG reflow surface is shown in *Fig. 7.*

4.2 Device characteristics

The current-voltage characteristics of the Nch FET and Pch FET are shown in *Fig. 8* and *Fig. 9,* respectively.

4.3 Application examples

Applications include the auto focusing IC reported separately in the special issue and various controller IC, custom memory, LED driver IC, etc. Building in of a photosensor and micro bump application, etc. are featured.

5. CONCLUSION

CMOS process technology centered about 6 μm and 2 μm CMOS technology was introduced above. The market demand for custom IC will expand its fields of application in the future. Fuji Electric is technology featuring built-in photo sensor, bump formation etc. based on the CMOS process technology developed up to here and its meeting the diversifying market demands.