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Bi-CMOS PROCESS TECHNOLOGY

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1. FOREWORD

Analog ICs are currently being made for high speed operation and in mixed-mode, analog-digital, configurations. Fuji Electric is involved in this trend and has developed a 2 μm rule Bi-CMOS process device. Bi-CMOS is an IC that combines Bipolar devices which are superior for high speed digital, analog, and high current output applications with CMOS devices which are noted for digital applications, low power consumption, and high packing density, on a single chip. The result is an IC that combines the merits of both devices.

Fuji Electric began to develop a 6 μm rule Bi-CMOS IC several years ago, and has continued to advance the technology to a point where device geometry in the 2 μm range has been developed. We have succeeded in perfecting a system on a single chip (system on chip) with high speed operation and the ability to perform a multitude of functions.

2. FEATURES OF THE TECHNOLOGY

2.1 Process technology

Fig. 1 shows a flow chart of the 2 μm rule Bi-CMOS fabrication process, and *Fig. 2* shows a cross section of the elemental devices.

The main features are shown below.

(1) Double metal- and single polysilicon- layer

We have made double metal layer and single polysilicon layer interconnects, making the most of flattening technology to make the surface level. In this way, we can eliminate diffused resistance, and achieve high speed operation, easier layout, and high packing density.

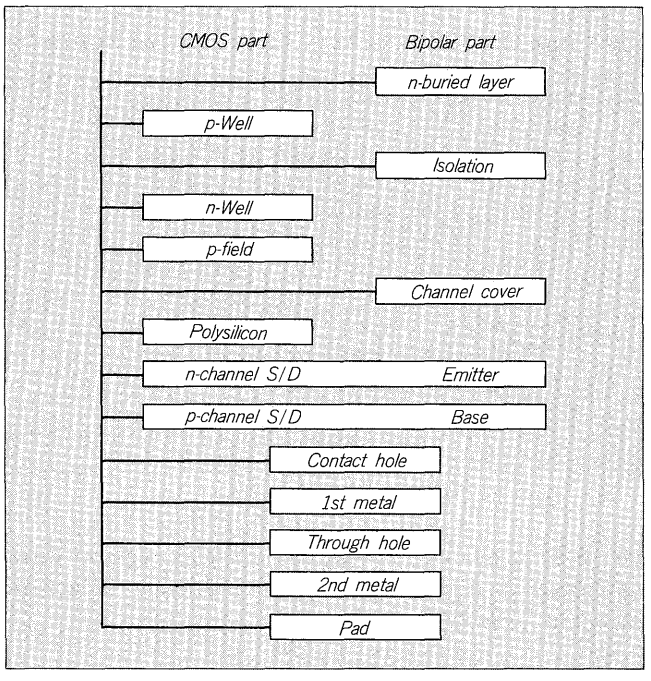
(2) Based on silicon-gate CMOS process

To standardize the process in order to use previously developed technology and equipment, the Bi-CMOS process is based on 2 μm rule CMOS technology. The bipolar part is integrated into the CMOS process with relative ease by changing a few steps.

(3) Process Simplification

The emitter of the bipolar npn transistor is made at the same time as the source/drain of the CMOS n-channel FET, and Arsenic is used as an impurity. The base is made at the same time as the source/drain of the CMOS p-channel FET, and Boron is used as an impurity. The drive-in process for both the base and emitter is done at the same time making use of the difference of diffusion constants of Arsenic and Boron. In this way, many steps within the CMOS and Bipolar fabrication can be combined and done at the same time, thus simplifying the process and reducing the number of steps.

Fig. 1 A flow chart of the 2 μm rule Bi-CMOS fabrication process



2.2 Properties of elemental devices

Planned specifications and actual results are shown in *Table 1*. Eighteen volt operation for the bipolar part, and 7V operation for the CMOS (digital) part is guaranteed. Below, the characteristics for each elemental device will be discussed.

(1) npn transistor

Fig. 2 A cross section of the elemental devices

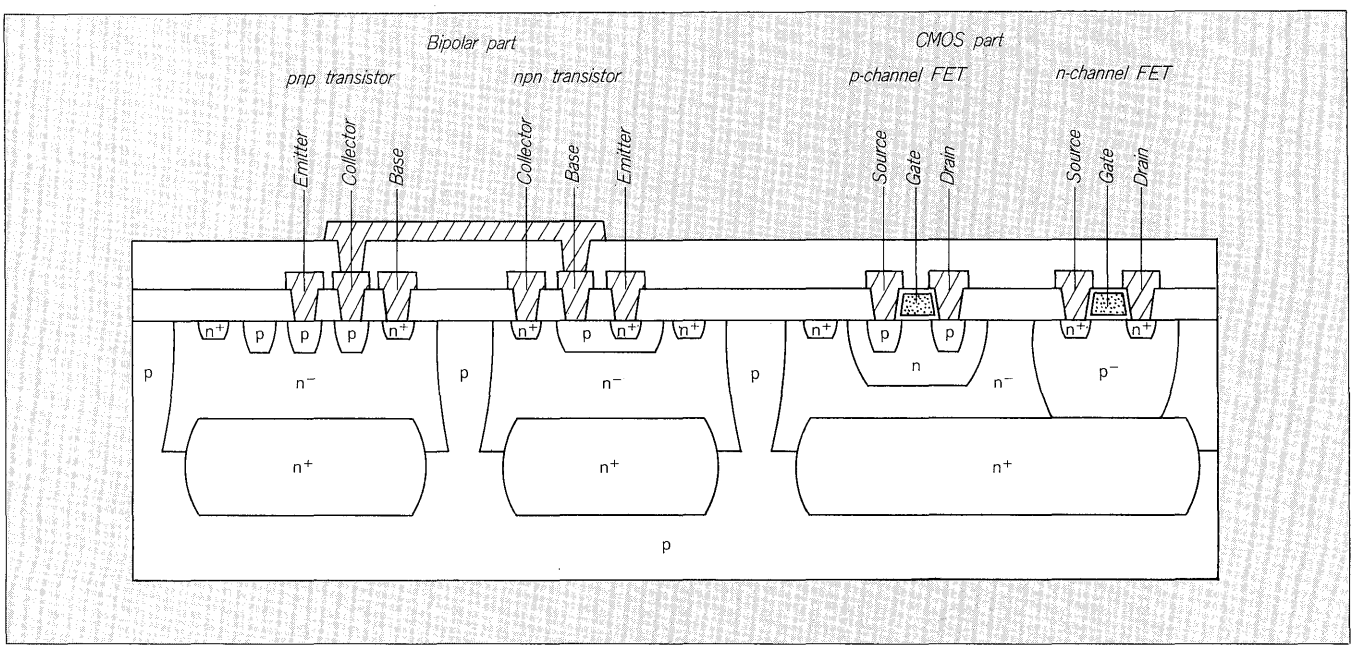


Table 1 2μm rule Bi-CMOS device characteristics

Element devices		Characteristics	Unit	Rule			Measurement value
				min	typ	max	typ
	p-channel MOSFET	V_{th}	V	0.5	1.0	1.5	1.2
		BV_{DSO}	V	10	15		17
		BV_{GSO}	V	10			>20
	n-channel MOSFET	V_{th}	V	0.5	1.0	1.5	1.0
		BV_{DSO}	V	10	15		14
		BV_{GSO}	V	10			>20
	npn-transistor	BV_{CBO}	V	20	30		29
		BV_{CEO}	V	20	30		30
		BV_{EBO}	V		5		4.5
		h_{FE}		50	80	150	70
		f_T	GHz	1	3		3
	npn-transistor	BV_{CEO}	V	20	30		27
		h_{FE}		10	20		27

Fig. 3 The h_{FE}-I_C characteristic for the npn transistor

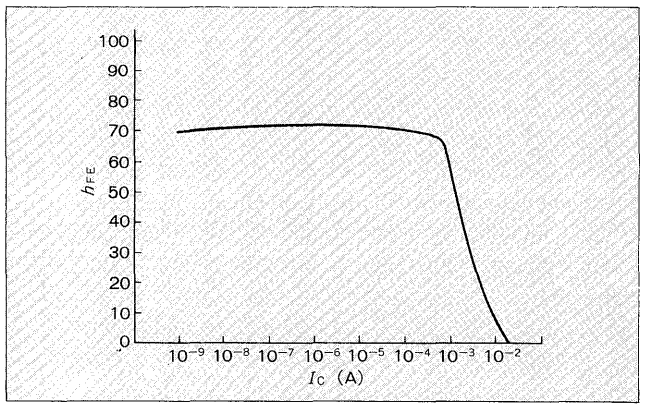
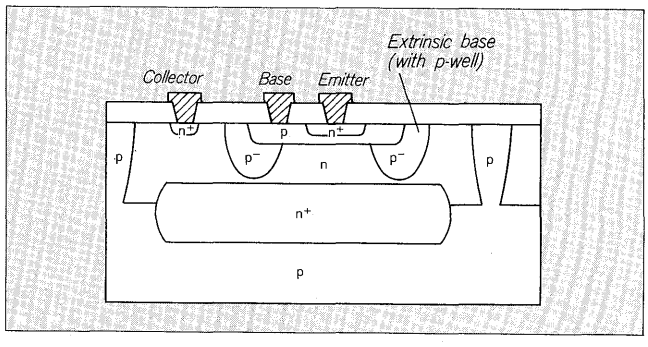


Fig. 4 A cross section of the high breakdown voltage npn transistor



The h_{FE}-I_C characteristic for the npn transistor is shown in *Fig. 3*. From I_C = 1nA to I_C = 1mA, h_{FE} remains constant for 6 figures, and proves that this Bi-CMOS process allows for few recombinations on the surface and in the depletion layer of both the base and emitter.

The breakdown voltage of the npn transistor is BV_{CBO} = BV_{CEO} = 30V at it shows that the curvature of the base diffused layer determines the avalanche breakdown voltage. In order to gain high breakdown voltages, we have already used the deeper profile, p-well diffusion, to cover the corner and to decrease the field intensity, as is shown in *Fig. 4*. Using this process we are able to gain in BV_{CBO} = 55V and BV_{CEO} = 40~50V.

(2) Lateral pnp transistor

The h_{FE}-I_C characteristics for lateral pnp transistors are shown in *Fig. 5*. In the case of lateral pnp transistors, the base transport factor, which is the ratio of the hole current reaching the collector to the hole current injected from the emitter, is the dominant factor. We find the fact that h_{FE} is proportional to the ratio of the emitter side

Fig. 5 The h_{FE}-I_C characteristics for the lateral pnp transistors

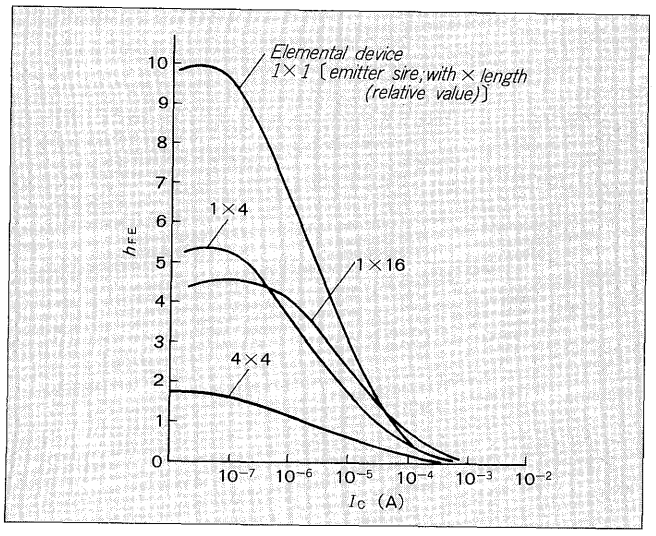
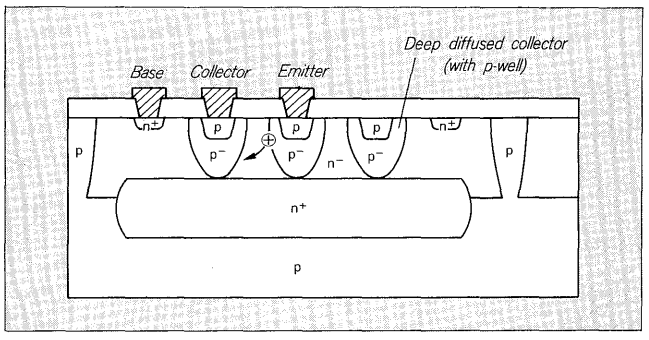


Fig. 6 A cross section of the lateral pnp transistor with deep diffused collector



area which faces to the collector to the whole emitter area. Especially, in the case of shallow junction, it is not appropriate to design the emitter as a circle with a large diameter or as a square with long sides, because it reduces the h_{FE}.

In order to reduce the h_{FE} of a parasitic pnp transistor whose collector is the substrate and the isolation layer, it is effective to design a deeply diffused collector to reduce the hole current from the emitter to the substrate, as is shown in *Fig. 6*. *Fig. 7* shows the reduction of the h_{FE} of a parasitic pnp transistor from 10 to 0.1 (1/100) due to a deep diffused collector. Thus we optimize both the device geometries and diffusion profiles.

(3) Schottkey transistor

A Schottkey transistor is an npn transistor with a Schottkey diode connected in a forward bias configuration between its base and collector. An equivalent circuit of a Schottkey transistor is shown in *Fig. 8*. The metal and n^- collector contact makes the Schottkey barrier and without using special metal such as platinum, we have developed both shallow junction contact and Schottkey contact by means of a special process technology. The forward biased characteristics for this Schottkey diode as compared with

Fig. 7 The h_{FE}-I_C characteristics for the parasitic pnp transistors

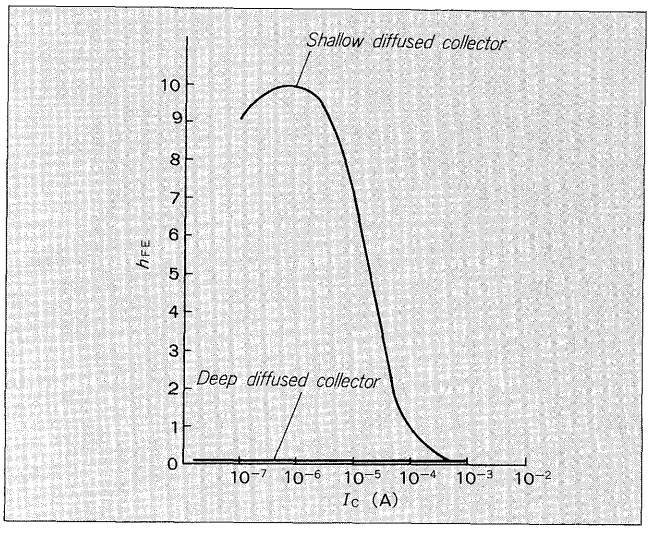
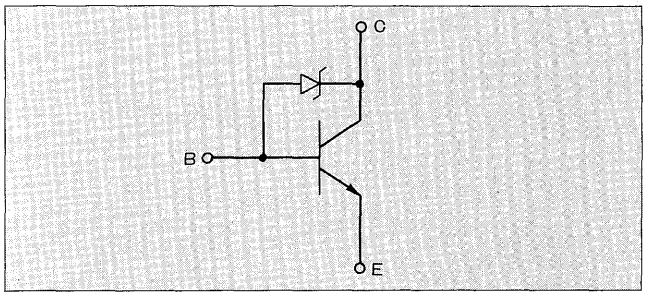


Fig. 8 An equivalent circuit of a Schottkey transistor



the base-collector forward biased diode is shown in *Fig. 9*.

(4) MOSFET

The I_D-V_{DS} characteristic for an n-channel MOSFET is shown in *Fig. 10*, and that for a p-channel MOSFET is shown in *Fig. 11*. The ratio of gate width to gate length, W/L, is 3.2/2.0 μm and 3.2/2.4 μm, respectively. Further the n-channel FET can achieve current values three times larger than that of the p-channel FET. This is due mainly to a difference in degree of mobility.

(5) Other devices

In addition to those devices mentioned above, vertical pnp transistors, Zenner diodes, condensers, and pinch-off resistors, etc. can be made. Using isolation diffusion, buried layer, and/or polycrystal silicon resistance, we can make ICs which are protected against static electricity. Also, latch-up free operation is made possible by using a low resistance buried layer.

2.3 Evaluation using TEG (Test Element Group)

We made TEGs of many circuit blocks, evaluated them, and confirmed their operation. This resulted in the following.

(1) Optimization of device geometries and process conditions.

(2) Confirmation of operation of middle scale ICs such as

Fig. 9 The forward biased characteristic for the Schottkey diode

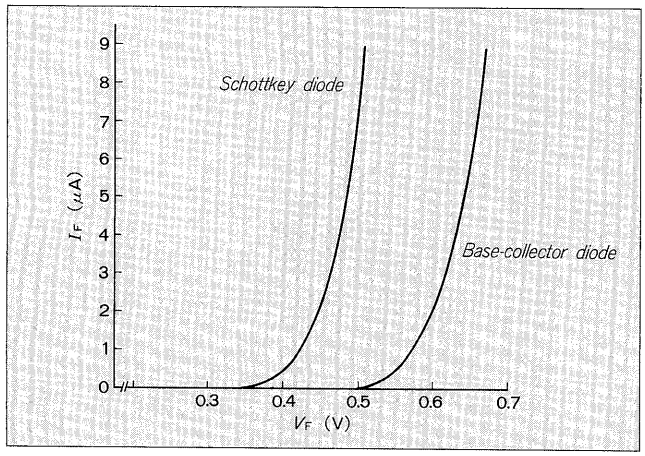


Fig. 10 The I_D-V_{DS} characteristic for an n-channel MOSFET

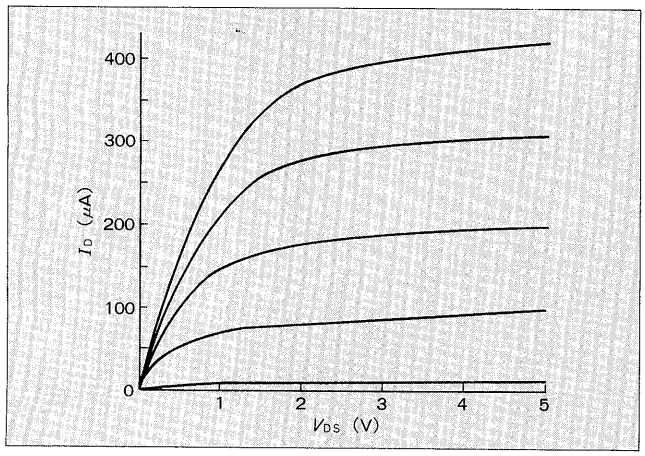
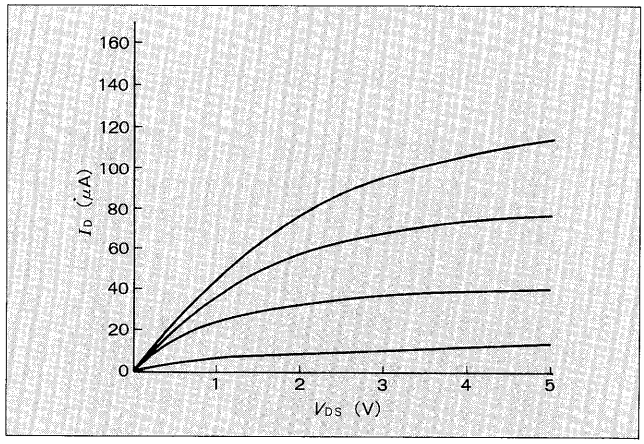


Fig. 11 The I_D-V_{DS} characteristic for a p-channel MOSFET



operational amplifiers.

(3) Confirmation of reliability.

Fig. 12 shows an example of a middle scale IC that was evaluated and confirmed using TEG.

Fig. 12 An example of a middle scale IC that was evaluated and confirmed using TEG

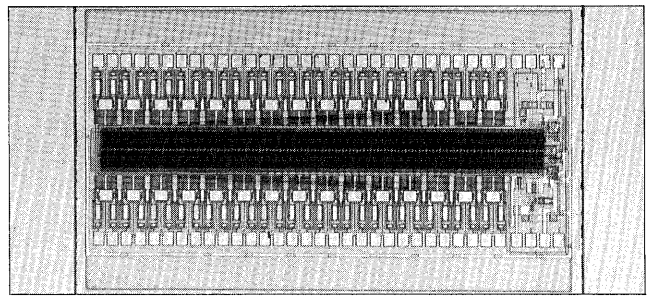
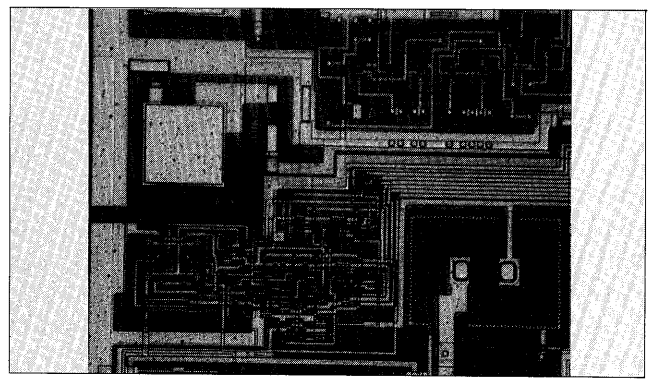


Fig. 13 A part of the IC that has been developed using 2 μm rule Bi-CMOS



2.4 Applications

One of the applications of the 2 μm rule Bi-CMOS is for analog-digital ICs. Especially promising applications are for A-D converters, disk drives, and video display controllers.

Fig. 13 shows a part of the IC that has been recently developed. In the lower left-hand corner there are logic circuits of CMOS devices, and in the upper right-hand corner there are analog circuits of bipolar devices. This is an analog-digital coexistant IC.

3. OTHER CONSIDERATIONS

The technology of 2 μm rule Bi-CMOS is suitable for multiple-function ICs and for system on chip. The freedom of designing circuits is great because various devices can be used. We consider it to be one of the best processes for ASICs (Application specific IC), as it meets the needs for customization and integration on one chip as well as the 6 μm rule Bi-CMOS process that has already been adopted.

From now, we shall apply CAD technology to CMOS cells, and the complete building up of sub-systems. We shall continue to improve the estimation technology in order to improve the functions of the devices. Both methods are used to shorten the TAT (Turn Around Time). Concerning the process technology, we plan to reduce the device geometry, to get faster operation, and to achieve higher packing density of devices for ICs.