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HIGH-VOLTAGE DMOSIC TECHNOLOGY

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1. FOREWORD

The rapid electronification of recent years has led to a strong demand for multi-functional, lower cost, faster, and smaller electronic systems. This is accompanied by an steadily increase in the role of the IC, their main component. Regarding the emission type flat panel display, printer, communication equipment, and automobiles, in particular, raising the performance and cutting the cost of high voltage IC which mount high voltage devices and low voltage logic circuits on one chip are important problems.

Following this trend, Fuji Electric has advanced development of high voltage IC technology and is now advancing this technology by increasing the voltage and current still further.

This article outlines the process and devices for 200V class and 400V class DMOS (Double Diffused MOS) IC technology as Fuji Electric's high voltage IC technology. It also introduces examples of application of this technology.

2. PROCESS TECHNOLOGY

2.1 200V class DMOSIC process technology

The 200V class DMOSIC process flow is shown in *Fig. 1*(a) and its cross-section is shown in *Fig. 2*. With this process, the low voltage CMOS section and high voltage devices: NDMOSFET, PDMOSFET, and NPN bipolar transistor can be formed on the same chip. The main feature of this process is that formation of the isolation layer and well, channel and base, and source drain and

Fig. 1 High-voltage DMOSIC process flow

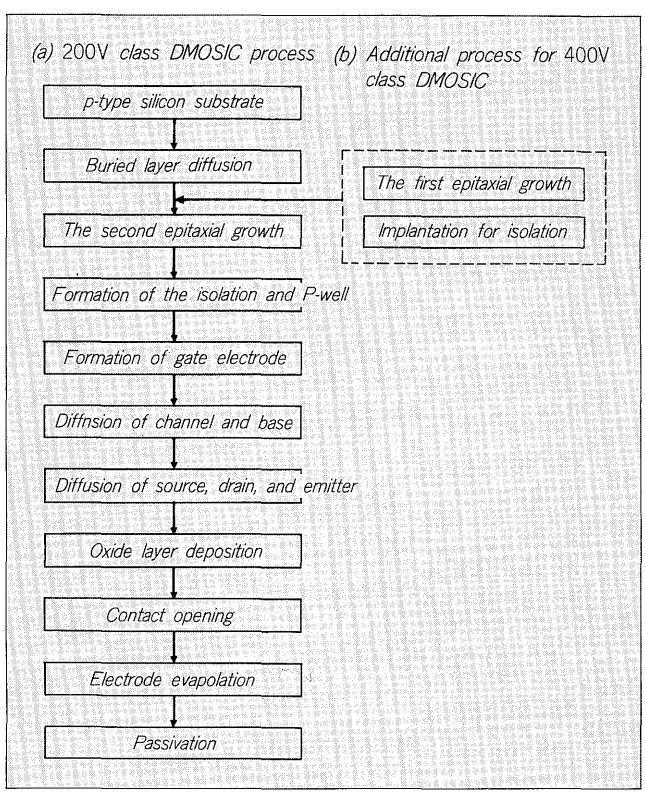


Fig. 2 Cross-section of 200V class DMOSIC

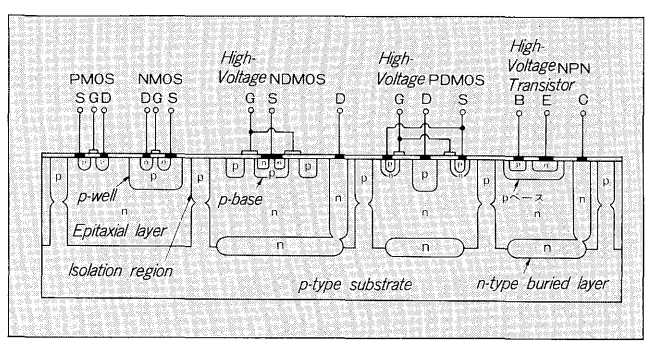
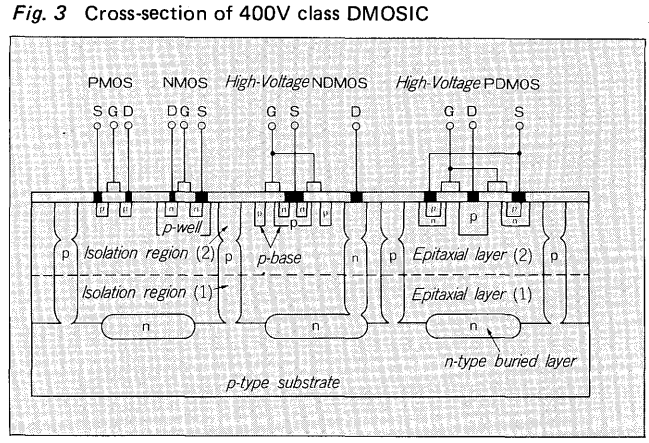


Fig. 3 Cross-section of 400V class DMOSIC



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2.2 400V class DMOSIC process technology

On the other hand, with the 400V class DMOSIC process, the isolation layer is formed by the double epitaxial method and high voltage is realized. As shown in *Fig. 1*(b), with the double epitaxial method, after the buried layer is formed, the first epitaxial layer is grown and the first isolation from the surface is selectively doped and after this, the second epitaxial layer is formed in the same manner as the 200V class process. The cross section of a double epitaxial DMOSIC is shown in *Fig. 3*. Since the isolation layer diffusion time is the same as that of the 200V class process, the depth of the diffusion layer is suppressed to the same degree as 200V class. Therefore, the isolation region is similar as in 200V class and the device area can be reduced. Because the thickness of the epitaxial layer (effective epitaxial layer) between the P base and buried layer can be made large, it is convenient for high voltages.

Table 1 High-voltage DMOSIC device characteristics

Element devices		Characteristics	Unit	Measurement value (typical)
200V class	NDMOS	BV_{DSO}	V	200
		V_{TH}	V	2.0
	PDMOS	BV_{DSO}	V	200
		V_{TH}	V	2.0
	NPN Transistor	BV_{CED}	V	100
		BV_{CBO}	V	200
		h_{FE}		100
400V class	NDMOS	BV_{DSO}	V	400
		V_{TH}	V	2.0
	PDMOS	BV_{DSO}	V	400
		V_{TH}	V	2.0
CMOS	NMOS	BV_{DSO}	V	25
		V_{TH}	V	1.0
	PMOS	BV_{DSO}	V	25
		V_{TH}	V	1.0

3. DEVICE TECHNOLOGY

3.1 200V class device

The device characteristics of 200V class high voltage devices and CMOS are shown in Table 1. The high voltage NDMOSFET has a current path from the drain to the source through the channel surface via the buried layer. Therefore, it is suitable for device with a large current capacity and higher blocking capability are realized by the source shape innovations, etc. described below.

The shape of the gate of a high voltage NDMOSFET is shown in *Fig. 4*.

By providing P^+ and N^+ source sections alternately at the source region with stripe-structure (stripe source), the contact area is reduced and the source region packing density and drain current are increased. The drain-source breakdown voltage (BV_{DS}) reduction is also prevented by providing a large radius of curvature at the end of the source region. *Figure 5* shows the relationship between the high voltage NDMOSFET BV_{DS} and drain current. Compared to the conventional type device with equal blocking capability and with the same device area, using the stripe source improves the current capacity.

On the other hand, the high voltage PDMOSFET is a lateral device which passes current from the source to the drain near the surface. Therefore, there is absolutely no leakage current generated to the substrate such as that of PNP transistors. The PDMOSFET maintains the breakdown voltage and reduces the on resistance by optimizing the impurity concentration and depth of diffusion of the drain region. For both of these high voltage decives, the channel is formed by the double diffusion method and punch-through in reverse blocking mode is prevented and the threshold voltage is suppressed to a low value.

Fig. 4 NDMOSFET structure with stripe-source

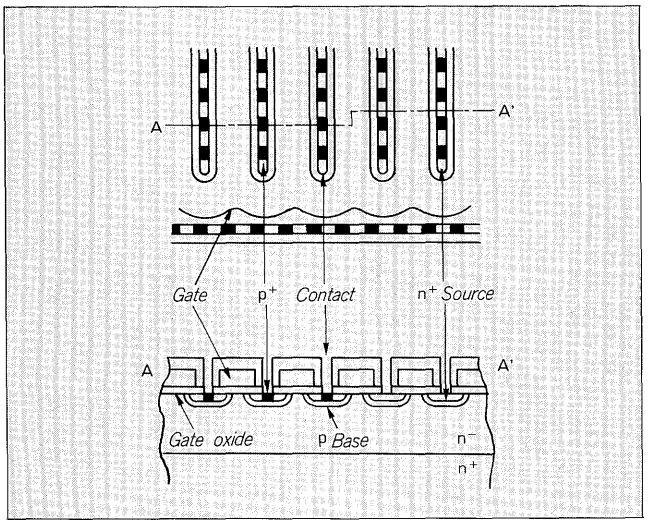


Fig. 5 Comparison between stripe-source and conventional source

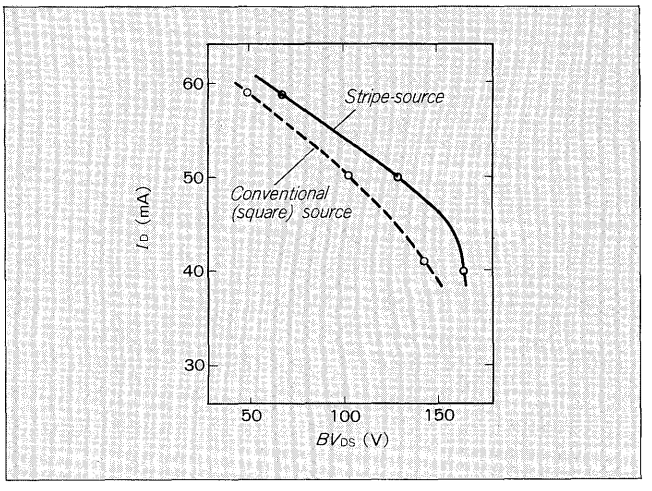


Fig. 6 I-V characteristics for 400V class NDMOSFET

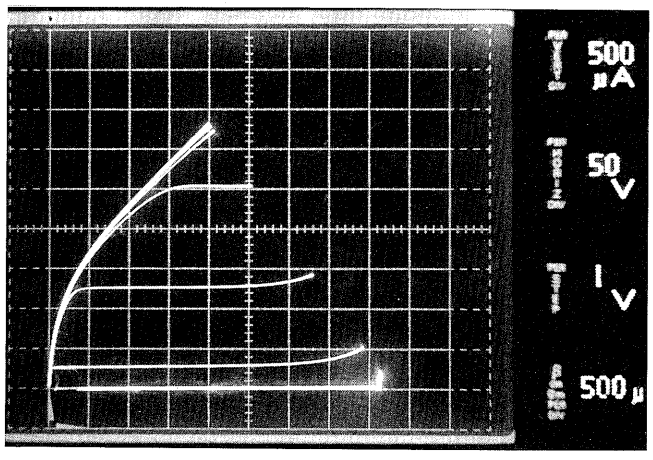
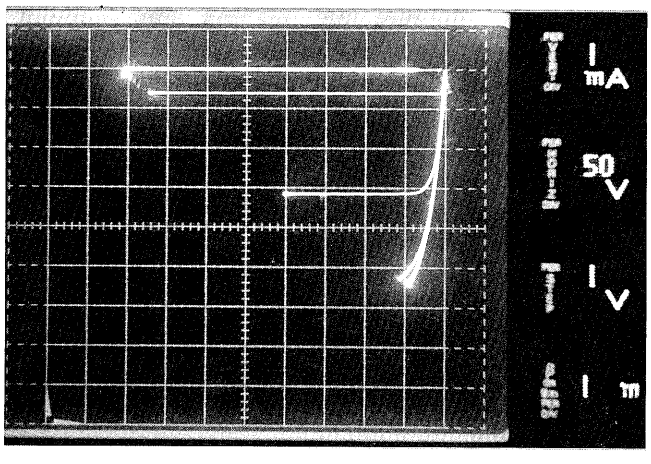


Fig. 7 I-V characteristics for 400V class PDMOSFET



The high voltage NPN transistor is described next. The high voltage NPN transistor realizes triple the current drive capacity of the high voltage NDMOSFET by using the DMOS structure and optimizing the emitter shape.

The low voltage logic circuit consists of a silicon gate CMOS and a 32-bit shift register operates at a maximum clock frequency of 10MHz.

3.2 400V class device

The device characteristics of a 400V class high voltage device are shown in *Table 1*. As previously described, the basic structure of the device is the same as that of a 200V class device, except for the use of the double epitaxial method.

The I-V characteristics of 400V class N and PDMOSFET are shown in *Fig. 6* and *Fig. 7*. A 400V class push-pull circuit can be formed on an IC chip by means of these devices.

Moreover, when realizing a 400V class device, the field plate structure and other high voltage technology to be described later are used.

When realizing a breakdown voltage exceeding 200V,

Fig. 8 CS-FP structure

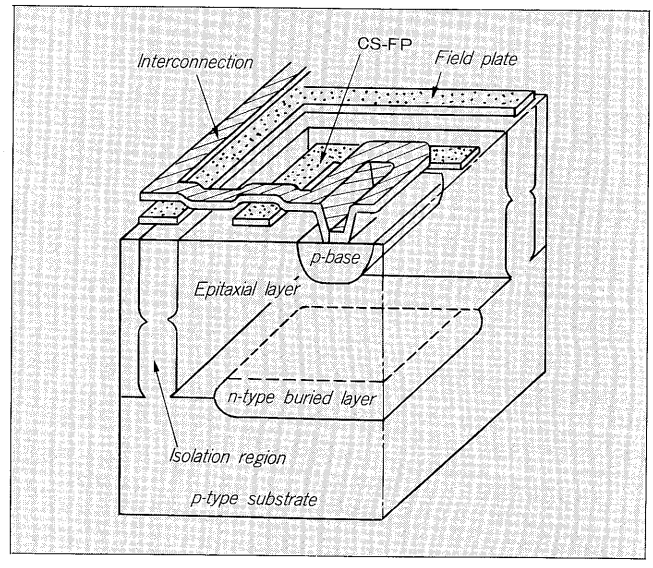
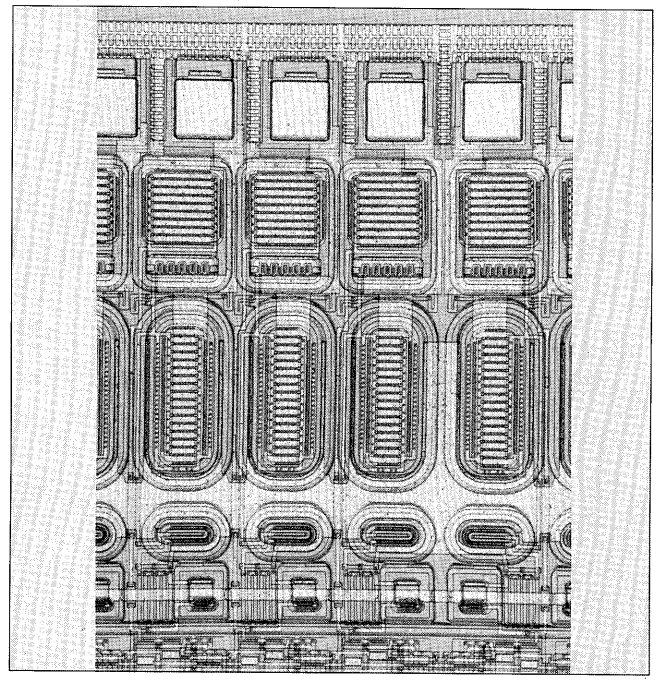


Fig. 9 Output circuits of flat panel display driver IC



electric field concentration is produced inside the device because of the high voltage interconnection and realization of a high voltage is prevented. Therefore, with 400V class high voltage devices, this is dealt with by forming a channel stopper (CS-FP) with the field plate shown in *Fig. 8*. When the CS-FP structure is used, the surface leakage current between the P base and isolation region is cut off and the depletion layer is spread to the epitaxial layer below the interconnection and therefore, electric field concentration can be avoided. This structure realizes a breakdown voltage improvement of approximately 30% over that of the conventional channel stopper that uses a diffusion layer.

4. HIGH VOLTAGE DMOSIC TECHNOLOGY APPLICATION EXAMPLES

The flat panel display driver IC is an example of application of these process device technologies. *Figure 9* shows the output section of the above IC using 200V class IC technology.

This circuit has a push-pull output circuit and the output section packing density is increased by employing an NDMOSFET that uses the stripe source previously described at the high side and low side devices. Moreover, a PDMOSFET is used to drive the high side NDMOSFET gate. This completely blocks operation of the parasitic PNP transistor between the PDMOSFET drain and P substrate and reduces the power loss.

5. CONCLUSION

Large current 200V class IC and 400V class IC technology have been established.

In the future, we plan to increase the capacity further and introduce fine process technology and make the control and output section faster and more densely packed and expect to open up new fields of application of the high voltage IC.