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POWER MOS FET

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1 INTRODUCTION

It has been quite a time now since Power MOS FET has been introduced and developed as an ideal power switching element in the market. During this period, in order to utilize to the full its high-frequency characteristics in a close interlink with application technology development policy while solving practical problems, we have come to expand the field of its application.

Technological innovation in semiconductor elements, as represented by development of ICs, is something remarkable, and this is applied also in the field of power devices. The problem of ON-resistance often cited as the weak point of Power MOS FET up to now is now being improved by application of fine pattern design and establishing of process technology. Further, the market expansion is directly connected with an increase in product amounts, and this triggers the lowering of the production cost. With the background of all these environments being materialized in a concrete form recently, the tendency of market expansion is rapidly accelerated so that there are many who believe that this year is really going to be the first year marking the "Power MOS FET Era".

Fuji Electric has been working together with Siemens of West Germany for making them to participate in Japanese market, and in order to achieve this goal, we have conducted our quality guarantee activities, mounting of parts in Japan and sales activities through Fuji Electronic Components, Ltd. This year, we have succeeded, further, in systematizing the wafer process in Japan, thus making ourselves more available for coping with the market demand. Here in this report, we like to introduce the series of the products, the subject of product designing along the trend of the technolgical innovation now as well as we will make a description of the module for coping with the tendency of making current larger and larger that came along with the expansion of field of application.

2 PRESENTING POWER MOS FET PRODUCT SERIES

Table 1 and *Table 2* show classified list of Fuji Electric's widely used products in Power MOS FET (SIPMOS FET) according to field of application.

Table 1 List of SIPMOS FET for general use (Driver, DC-DC converter, DC motor, inverter, etc.)

Type	Outer view	Main rating		
		V_{DS}(V)	I_D(A)	R_{DSON}(Ω)
BUZ71	TO220	50	12	0.1
BUZ71L	TO220	50	14	0.1
BUZ11HA	TO220	50	25	0.055
BUZ11	TO220	50	30	0.04
2SK562	TO3P	50	39	0.04
BUZ72	TO220	100	10	0.20
2SK564	TO3P	100	32	0.06
BUZ73A	TO220	200	5.8	0.6
BUZ31	TO220	200	12.5	0.2
2SK616	TO3P	200	22	0.12
EUF02-030	TO3P	300	20	0.15
EUE03-050F	TO3P	500	9	0.8

Table 2 List of SIPMOS FET for switching power supply

Type	Outer view	Main rating		
		V_{DS}(V)	I_D(A)	R_{DSON}(Ω)
BUZ76A	TO220	400	2.6	2.5
BUZ60	TO220	400	5.5	1.0
BUZ74A	TO220	500	2.0	4.0
BUZ41A	TO220	500	4.5	1.5
2SK724	TO3P	500	10	0.67
2SK565	TO3P	500	9.6	0.6
2SK725	TO3P	500	15	0.38
BUZ78	TO220	800	1.5	8.0
BUZ80	TO220	800	1.6	4.0
2SK566	TO3P	800	2.9	4.0
EUD04-080	TO3P	800	2.3	2.0
EUC05-090	TO3P	900	5 (3)	4.5
EUD06-090	TO3P	900	(5)	2.3
BUZ50B	TO220	1,000	2.0	8.0

3 DESIGNING OF POWER MOS FET

As Power MOS FET (n channel) operate with a single carrier (electron), no conductivity modulation is provided. So that it has a drawback of larger voltage drop in comparison with that of bipolar devices. In order to reduce this ON-resistance, it is necessary to (1) reduce ON-resistance of unit MOS FET and (2) increase the number of its cells (that is, miniaturization of cell dimension). On the other hand, there is a reciprocal relation between withstanding voltage (BV_{DSS}) and ON-resistance. Fuji Electric is trying to establish an optimum designing and process taking special attention of the following points.

(1) Edge structure and passivation of voltage blocking parts.
(2) Optimum doping profile in the high-resistance drain region.
(3) Optimization of cell size
(4) Application of fine pattern technique to power devices.
(5) Development of clean process and getting technique for improving the gate withstanding voltage distribution and the yield.

3.1 Improvement of ON-resistance

Fig. 1 shows ON-Resistance component of power MOS FET. This can be expressed by the following formula:

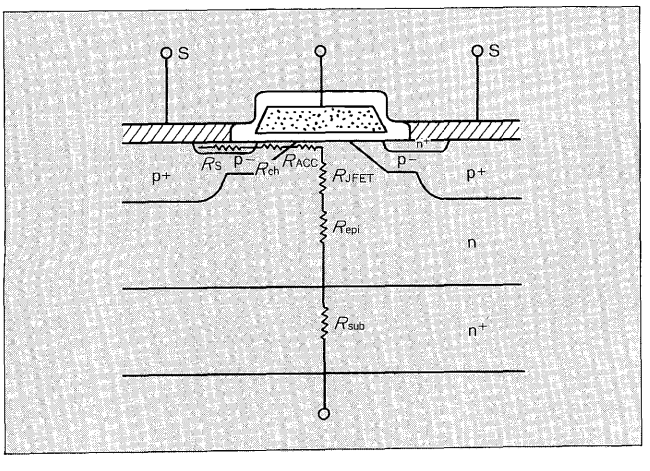
$$R_{on} = R_s + R_{ch} + R_{ACC} + R_{JFET} + R_{epi} + R_{sub}$$

whereas,

R_s : Resistance of source region
R_{ch} : Resistance of channel part
R_{ACC} : Resistance of accumulation layer
R_{JFET} : Resistance of JFET part
R_{epi} : Resistance of high-resistance drain region
R_{sub} : Resistance of substrate

Here, R_s and R_{sub} are neglibibly small. Supposing the current flows as shown in *Fig. 2*, each component for square cell can be expressed as follows[1].

Fig. 1 Component of power MOS ON-resistance



(1) R_{epi}: Resistance of epitaxial high-resistance drain layer, For resistance

$$R_{epi} = r_{epi} \times \frac{\rho \cdot W}{(S+a)^2}$$
$$= \frac{\rho \cdot W}{(S+a)^2} \times \left[1 - \frac{W'}{W} + \frac{S+a}{4W}\right.$$
$$\left. \ln \frac{(S+a)-(S'-2W')}{(S+a)+(S'-2W')} \times \frac{(S+a)+S'}{(S'+a)-S'}\right] \quad \text{..... (1)}$$

(2) R_{JFET}: Resistance due to narrowing of current passage by JFET between p- layers.

$$R_{JFET} = \rho \cdot W_j \frac{S+a}{4} \cdot \ln\left[\frac{a}{2S+a} \cdot \frac{S+a+S'}{S^2+a-S'}\right] \text{ .. (2)}$$

(3) R_{ACC}: Resistance of accumulation layer in high-resistance drain region immediately under the gate

$$R_{ACC} = \frac{1}{8C_{ox}\mu_n (V_g - V_{FB})} \times \frac{(S+a)^2}{a(a+2S)} \cdot$$
$$[(S+a)^2 \cdot \ln(1+\frac{a}{S}) - as - \frac{a^2}{2}] \quad \text{..... (3)}$$

whereas,

C_{ox} : Gate capacitance
μn : Electron mobility within accumulation layer
V_g : Gate voltage
V_{FB} : Flat band voltage on drain region

(4) R_{ch}: Resistance of channel part

$$R_{ch} = \frac{(S+a)^2}{4 \cdot S} \cdot \frac{L}{\mu_{ni} C_{ox}(V_g - V_{th})} \quad \text{..... (4)}$$

μ_{ni} : Electron mobility within channel (inversion layer)
V_{th} : Threshold voltage
L : Channel length

Fig. 3 and *Fig. 4* show each component of ON-resistance and dependency on cell interval of ON-resistance according to withstanding voltage class. As it is clearly seen

Fig. 2 Hypothetical current flow in one cell

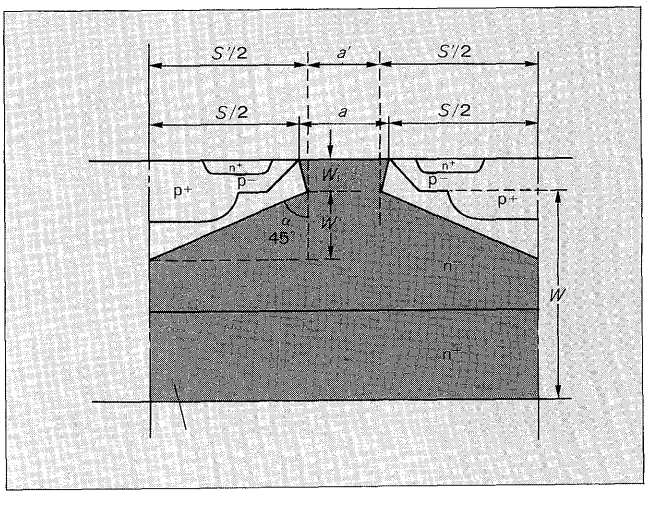


Fig. 3 Comparison of ON-resistance components (500-V class)

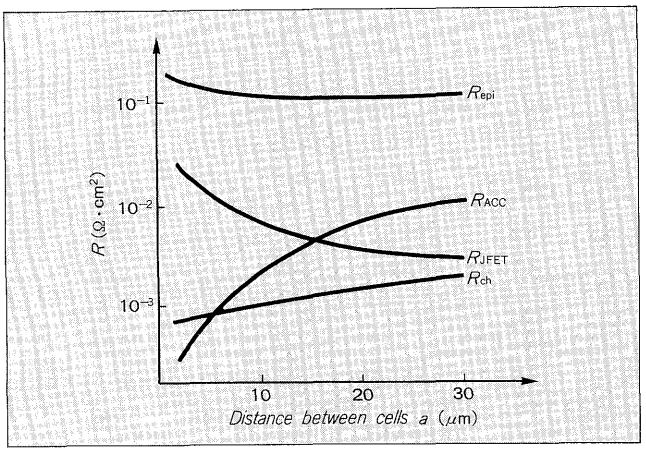
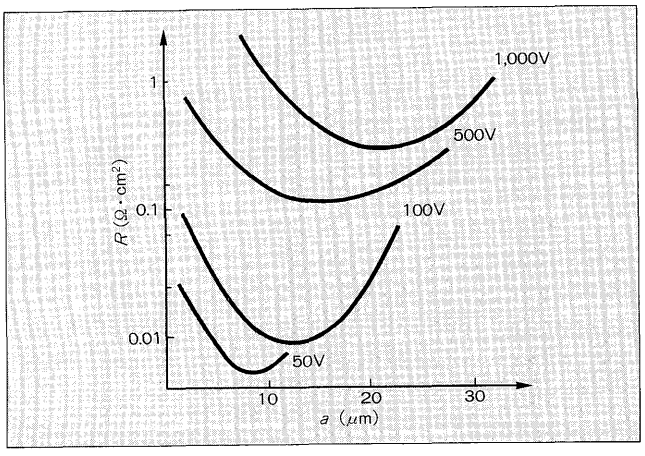


Fig. 4 Relationship between cell interval and ON-resistance



from the figures, there is certain optimum value for distance between cells in each withstanding voltage class.

Furthermore, by seeking the doping profile of high-resistance drain region that maximizes the withstanding voltage and, yet, minimizing the ON-resistance, it is realized in the double epitaxial layer. Miniaturization of cells as much as possible is endeavored through optimization of cell dimensions for the high withstanding voltage (200 to 300 V or more) elements, and as for the lower withstanding voltage (equal or less than 100 V) elements, improvement of process technique.

3.2 Improvement of withstanding voltage and its stabilization

The withstanding voltage of planer device as power MOS FET, when it is seen from the relation (*Fig. 5*) between specific resistance in an ideal case and its withstanding voltage, the realizable value will be about 50 to 70%. An effort is taken so as to approximate as much as possible to the ideal value through optimization of edge structure and passivation. Fuji Electric has also achieved the high withstanding voltage by optimizing the field plate structure by poly-silicone resistance or metal one and guard rign structure, and further, by utilizing resistive insulating

Fig. 5 Relationship between specific resistance and planer withstanding voltage

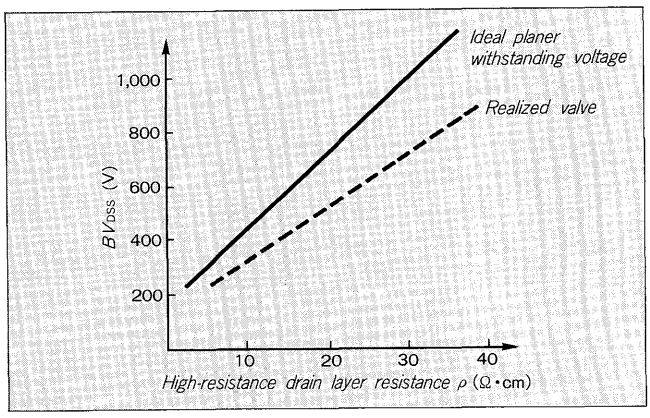
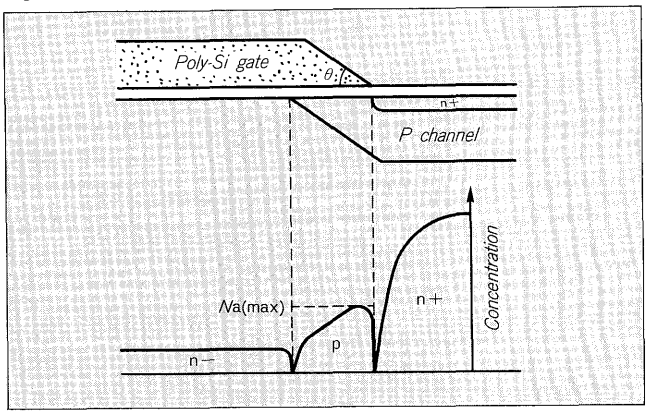


Fig. 6 Concentration distribution in channel part



film for stabilization's sake.

3.3 Control on gate threshold voltage (V_{th});

The value of V_{th} is determined by the maximum surface concentration within the channel part obtained by ion implantation method. *Fig. 6* shows the concentration distribution of the channel part. When V_{th} is calculated from this, V_{th} will be different by its position and is determined by the formula (4).

$$V_{th}(x) = \phi_{ms} + 2\phi_F - \frac{Q_{ss}}{C_{ox}} + \frac{\{4\epsilon_s \rho N_a(x)\phi_F\}^{1/2}}{C_{ox}} \quad \cdots\cdots (5)$$

Here, $N_a(x)$ represents the concentration distribution in the channel. The maximum value of V_{th} takes place where $N_a(x)$ is the largest. In order to manufacture V_{th} with least possible fluctuation, it is necessary that the source retion should be taken as shallow as possible so as not to vary the maximum channel concentration value and, at the same time, channel also should be as shallow as possible, so as to improve the diffusion controlability.

In Fuji Electric, by utilizing the variation of etching rate due to damage by ion implantation, we have attained the control on taper etching of the gate with good reproductivity and brought out optimization of channel

length and source depth, obtaining characteristics with extremely few fluctuation.

Fig. 7 shows the relationship between channel part dosis and V_{th}. V_{th} can be controlled in a large scale only by changing taper angle.

3.4 Improvement of distribution of gate resistance to breakdown voltage

Breakdown of gate oxide by static electricity or over-voltage presents a big problem for MOS FET. Fuji Electric improves the distribution of rupture withstanding voltage by taking up the good ixidation forming technique with fine quality layer with little defects as pinhole and others and reduces variation of quality. *Fig. 8* shows distribution of gate oxide disruptive field distribution by process method. The aim of improvement is optimization of gas at the time of placing of oxide, and that of conditions as temperature and others, as well as optimization of HCI oxidation and improvement of wafer clean degree level.

3.5 Improvement of breakdown resistance

As Power MOS FET operates in high frequency, spike voltage tends to generate due to L load application and floating inductance, and in extreme cases, a voltage may sometimes impressed surpassing BV_{DSS}. Also, a breakdown due to displacement current $C \cdot \frac{dV}{dt}$, at the time of turn-off has to be considered. Fuji Electric has realized designs taking into full account of these points. As for the mechanism to be broken down, as shown in *Fig. 9*, for example, when a voltage is applied with a load L, surpassing BV_{DSS}, avalanche multiplied hole current with run into p^+ well or p^- channel, passing through p diffusion resistance R_b, directly below n+ source, flows to source electrode. At this time, when the voltage drop ($J_p \times R_b$) caused by the hole current J_p is larger than the diffusion potential between n^+ source and p^- channel (about 0.6 V), parasite bipolar transistor (n^+ [source]-p-n^-) is energized and implants electrons into delpletion layer, and this drops abruptly the holding voltage, letting a large current flow and, in the end, overall breakdown is caused[5]-[6]. Likewise, as for the dV_{DS}/dt capability components by avalanche multiplied current and displacement current are added and the parastic transistor will operate under the following conditions[7].

$$0.6 \leqq \frac{1}{\left(\frac{BV}{BV_{DSS}}\right)^4 - 1} \cdot (R_{ext} + R_b) I_{Dsat} + (R_{ext} + \frac{1}{2} R_b) \cdot C_{gd} \cdot \frac{dV_{DS}}{dt} \quad \cdots\cdots\cdots (6)$$

The first term on the right is due to avalanche current and the second, to displacement current.

From the above, it is obvious that in order that an improvement should be brought, it is necessary to

Fig. 7 Relationship between channel dosis and V_{th}

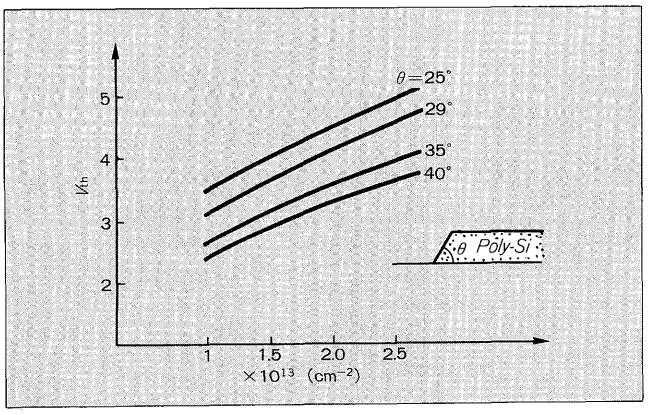


Fig. 8 Gate breakdown capability and gate oxide processing method

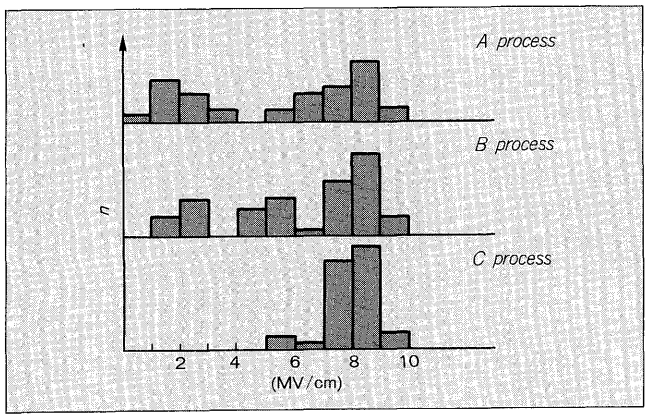


Fig. 9 Avalanche current flow at the time of breakdown

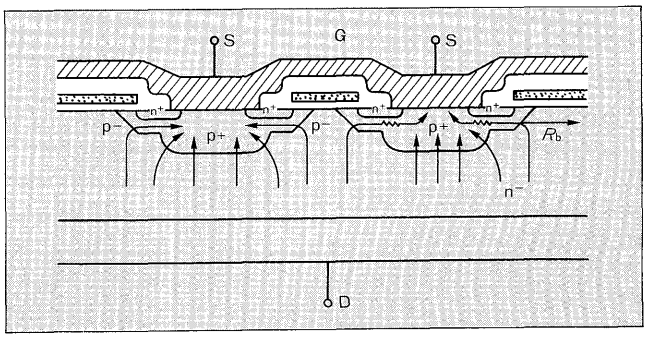
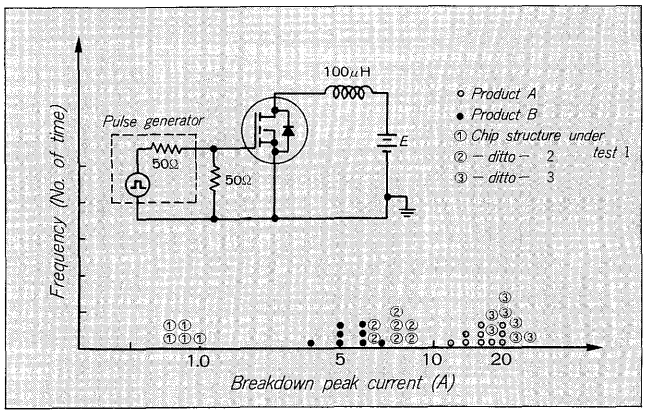


Fig. 10 L load capability of power MOS FET



(1) Decrease R_b,
(2) Let avalanche hole current pass as much as possible through p^+ region.
(3) Decrease C_{gd} (reduction of displacement current).
(4) Unifying of electric field distribution at the time of avalanche breakdown
(5) Unifying of current distribution at the time of transitory response.

And these are what we are effectuating in order to obtain the improvement.

Furthermore, we have made a through research on the temperature distribution in the MOS FET chips under operation, and we apply the results of the research to bring solutions against local concentration of current, thus the breakdown resistance capacity is much improved.

Fig. 10 shows the experiment data on the relation between L load resistance and chip structure. As we have seen, we have also developed elements that can cope with severe requirements on L load capability.

3.6 Future plans

(1) Making low-voltage class products into super-low-on resistance.
(2) Reduction of gate threshold voltage and increase of g_m ($V_{th} \leqq 2.0$ V)
(3) Reduction of reverse recovery time of inherent diodes ($t_{rr} \leqq 200$ ns).
(4) Mass production of high withstanding voltage of 900 V and 1,000 class products
(5) Obtainment of faster switching (reduction of input capacity, decrease of gate resistance)
(6) Reduction of V_{th}, g_m and R_{on} fluctuation

Our plans for immediate future are to bring solutions to the above mentioned problems at an earliest possible date, to expand the product series and, at the same time, through improvement and optimization of cell size and edge structure, to carry out further miniaturization of chips and improvement of our process technique up to still higher level.

4 MOS FET MODULE

When high power current is desired to handle, generally, individual elements are mounted in parallel to control high power current. In this case, naturally, when the current to be handle gets more and more powerful, the number of elements required to be connected in parallel will also become more. And this wiring interconnecting each element is the enemy of the effort of making it high frequency, and we should take a particular care of transient drain current unbalance caused at the time of turning on and turning off of each element and the surge voltage produced by the wiring induction components and current fluctuation.

The MOS FET Module introduced here in this report has the structure incorporating as much as possible the two ideas mentioned above without modifying in a large scale the foundamental appearance of conventional bipolar transistor module.

4.1 Module series

Table 3 shows the series of MOS FET Modules. By connecting fast recovery diodes whose reverse recovery time is less than 100 ns in parallel with MOS FET, faster switching is obtained.

The adopted outer view has the following features: dimensions for mounting to coolant is 93 mm which is as big as that of 75-A class bipolar transistors. Then, its main output terminal has two sets of MOS FET, independent one from another, so that they can be used for both receiving power supply and for inverter. The outer view is as shown in *Fig. 11*.

4.2 Features of modules

Main factors that give a large influence to transient current unbalance and surge voltage when MOS FET is turned on and turned off are classified and indicated in *Table 4* above. *Fig. 12* and *Fig. 13* show the turn-on current flowing to 6 parallel-connected FETs (2SK565) when internal wiring is changed under test, and as it is obvious from the figures, the influence caused by induction components generated by a small difference in dimensions plays a big role.

Fig. 11 MOS FET module

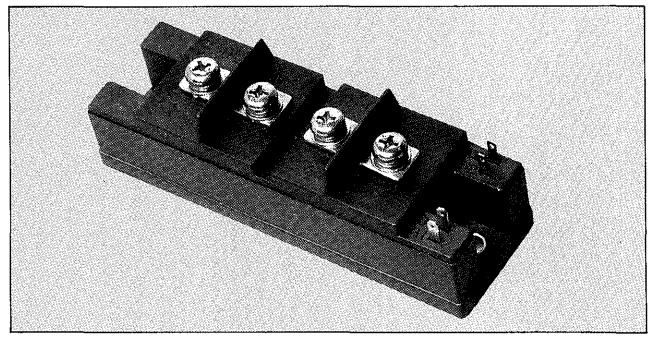


Table 3 List of MOS FET module series

Reverse recovery characteristic of FRD	Rated current / V_{DSS}	35 A	50 A
Low-speed type	450 V	2M135F-045	2M150S-045
	500 V	2M135S-050	2M150S-050
High-speed type	450 V	2M135F-045	2M150F-045
	500 V	2M135F-050	2M150F-050

Table 4 Points to be considered for parallel operation with MOS FET

Transitory state / Factor	Wiring	MOS FET characteristics
Turn on	Large influence to current balance	Determined more or less by forward conduction characteristics.
Turn off	Large influence to surge voltage	

Fig. 12 Turn on current balance when wiring connection is imperfect

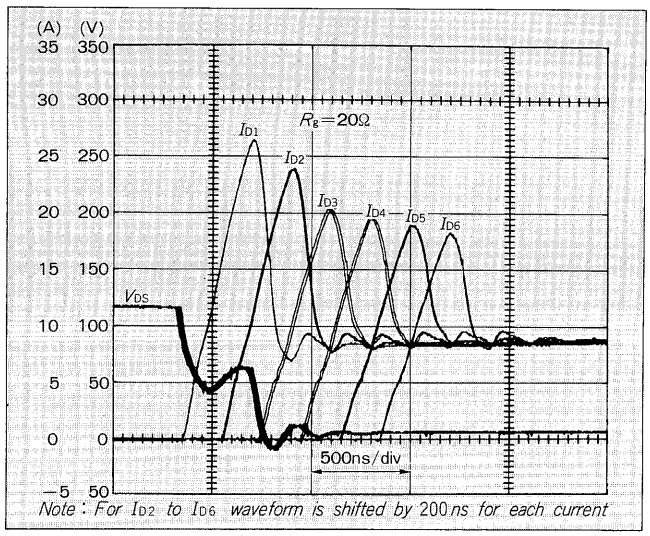


Fig. 13 Turn on current balance when wiring connecting is good

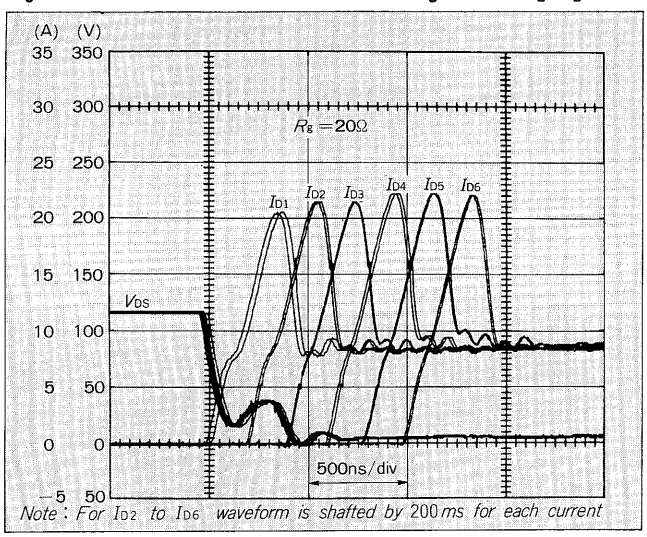
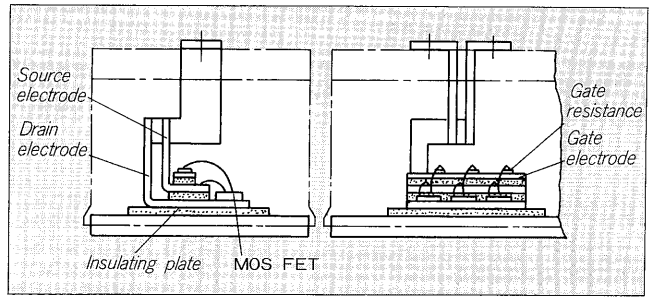


Fig. 14 shows a module structure that has realized a stable operation during the transitory state by reducing as much as possible the induction components in the internal wiring.

Fig. 14 Outline of internal structure of module (patent pending)



4.3 Some technical subjects

Some technical subjects we are facing are the following.

(1) Reduction of thermal resistance of the insulating plate.
(2) Devices for package coping with high frequency.
(3) Reduction of driving power
(4) Compoundation

The current rating of MOS FET is determined by heat radiating conditions and when higher frequencies are required the more, the more the mechanical construction suitable for mounting on equipment will be required and futher when number of elements in parallel connection is increased and the more the frequencies will be available, the drive mechanism will become more complex and as the whole, modules with better efficiency are required and the development of compoundation technique in order to incorporate an optimum drive circuit will be sine qua non.

Bibiography:

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