“Super J-MOS” Low Power Loss Superjunction MOSFETs

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ABSTRACT

Fuji Electric has developed superjunction MOSFETs with an optimized surface design that delivers lower switching loss. In these “Super J-MOS”chips, gate length and channel density were adjusted to optimize the gate-to-drain capacitance and threshold voltage, thus achieving lower turn-off loss. For devices rated at 600 V/20 A/0.19 □, an extremely low turn-off loss of 160 μJ at the turn-off dV/dt of 10 kV/μs was realized. Power efficiency is over 94.0%, enabling compliance with the 80 PLUS certification.

1. Introduction

Recently, in response to heightened interest in global environmental protection through conserving energy and reducing CO_2 emissions, lower levels of power loss are sought in so-called IT equipment, such as PCs and servers. In order to reduce the power loss in IT equipment, the power conversion devices used in IT equipment must be made more efficient, and the technology that enables this higher efficiency is power semiconductors.

The power semiconductors installed in power conversion equipment operate as switching devices, and their power loss consists of conduction loss while the device is in its on-state, and switching loss when the device changes from its on- to off-state or from its off- to on-state. To achieve higher efficiency and lower loss in power conversion equipment, both types of loss must be reduced.

This paper reports on Fuji Electric’s successful development of a “Super J-MOS” (Superjunction MOSFET) that achieves low switching loss as a result of optimization of the SJ-MOSFET surface structures from a theoretical perspective and an improved trade-off relationship between turn-off loss E_{off}, generated when the device changes from its on- to off-state, and the value of turn-off dV/dt, which indicates the time-change of drain-to-source voltage at the time of turn-off.

2. Characteristics of the “Super J-MOS”

The use of an SJ-MOSFET is one way to reduce both conduction loss and switching loss. Compared to a conventional power MOSFET, the SJ-MOSFET features a significantly improved trade-off relationship between the device breakdown voltage BV_{DSS} and the specific on-resistance $R_{on}\cdot A$, and because the conduction loss can be reduced dramatically, SJ-MOSFETs are being used more and more in power conversion equipment.

Figure 1 shows schematic cross-sectional views of a SJ-MOSFET and a conventional MOSFET. The SJ-MOSFET has a structure in which p-pillars and n-pillars are arranged alternately in the drift region. By narrowing the width of each pillar, the impurity concentration in the drift region can be increased without decreasing the breakdown voltage, and therefore the on-resistance can be reduced.[(1)~(4)]

Furthermore, because an SJ-MOSFET has signifi-

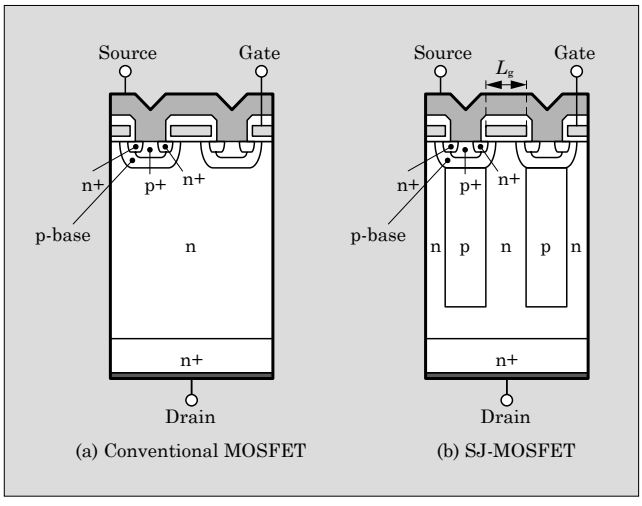

Fig.1 Schematic cross-sectional views of power MOSFETs

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*1: Miller period: See supplemental explanation 2 on page 88.

cantly smaller $R_{on}\cdot A$ than a conventional MOSFET, its gate-to-drain capacitance C_{GD} is also significantly smaller. As a result, there is a problem of the C_{GD} becoming too small, causing the gate controllability to decrease and the turn-off dV/dt to increase. Additionally, if the gate resistance R_g is increased in order to reduce the turn-off dV/dt, the Miller period*1 will lengthen and the loss will increase. As a result, the tradeoff relationship between E_{off} and turn-off dV/dt deteriorates. Accordingly, if the tradeoff relationship between E_{off} and turn-off dV/dt can be improved, and the turn-off loss decreased, a low power loss device that realizes both low conduction loss and low switching loss can be realized. In fact, the Super J-MOS is a realization of such a device.

3. Optimization of Surface Structures

3.1 Design concept

In order to improve the tradeoff relationship between E_{off} and turn-off dV/dt in a SJ-MOSFET, it is necessary to reduce turn-off dV/dt under conditions of constant R_g. Focusing on the reduction of turn-off dV/dt, characteristics of the tradeoff between E_{off} and turn-off dV/dt were improved in accordance with the following equation.

Assuming that the gate-source capacitance during turn-off is constant within the Miller period, turn-off dV/dt can be expressed as in Eq.(1).

$$\frac{dV}{dt}=\frac{\frac{I_D}{g_{fs}}+V_{th}}{C_{GD}\cdot V_{DS}\cdot R_g} \quad \cdots\cdots(1)$$

I_D : Drain current
g_{fs} : Transconductance
V_{DS}: Drain-to-source voltage

From Eq.(1), it can be understood that when R_g, I_D and V_{DS} are constant, increasing C_{GD} and decreasing the threshold voltage V_{th} are effective for reducing turn-off dV/dt. C_{GD} is determined by the distance between the p-bases, i.e., the gate length L_g, and therefore L_g should be lengthened in order to increase C_{GD}. Moreover, because V_{th} is determined according to the impurity concentration of the p-base region, V_{th} can be decreased by reducing the impurity concentration of the p-bases.

3.2 Gate length dependence of turn-off loss

Simulations based on the design concept were performed to estimate the L_g dependence of E_{off}. Figure 2 shows the L_g dependence of E_{off} and turn-off dV/dt. E_{off} values are shown for the case that turn-off dV/dt is 10 kV/μs, and turn-off dV/dt values are shown for the case that R_g is 91 Ω. Additionally, the values of L_g are relative to the value of L_g prior to optimization of the structure.

As shown in Fig. 2, turn-off dV/dt can be reduced by lengthening L_g, and the resulting decrease in the value of E_{off} was confirmed. When L_g increases above 1.4, the E_{off} value shows nearly no improvement and remains nearly unchanged. This is thought to be caused by the lengthening of the Miller period and increased loss that occurs when C_{GD} is increased, causing the turn-off time to become longer and the feedback capacitance to increase.

3.3 Threshold voltage dependence of turn-off loss

Next, the V_{th} dependence of E_{off} and turn-off dV/dt was calculated. The results are shown in Fig. 3. As in the calculation of the L_g dependence, the values of V_{th} are relative to the value of V_{th} prior to optimization of the structure. Additionally, an estimation of the V_{th} dependence was calculated based on the simulation described in Section 3.2 and using an optimal L_g design value of 1.4.

As shown in Fig. 3, turn-off dV/dt decreases as V_{th} becomes smaller, and accordingly, a decrease in the value of E_{off} was confirmed. If V_{th} becomes too small, however, a problem may occur in which the device turns-on unintentionally due to noise. In optimizing the design for V_{th}, it is necessary to be careful so as not to reduce V_{th} too much in order to prevent malfunction of the device.

Based on the above results and using L_g=1.4 and V_{th}=0.75 as optimal structure values, the tradeoff rela-

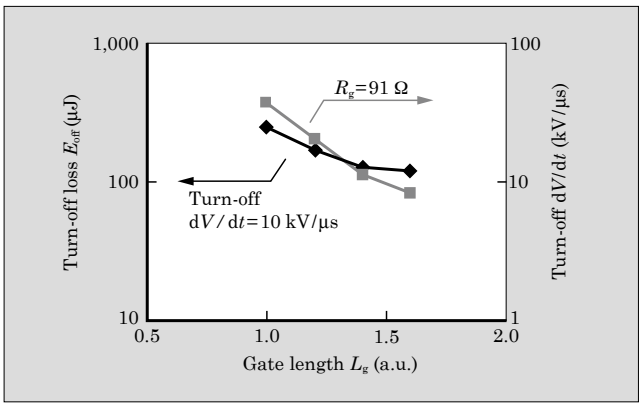

Fig.2 L_g dependence of E_{off} and turn-off dV/dt

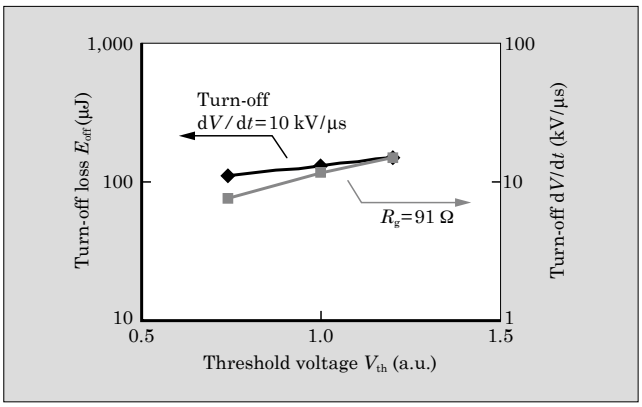

Fig.3 V_{th} dependence of E_{off} and turn-off dV/dt

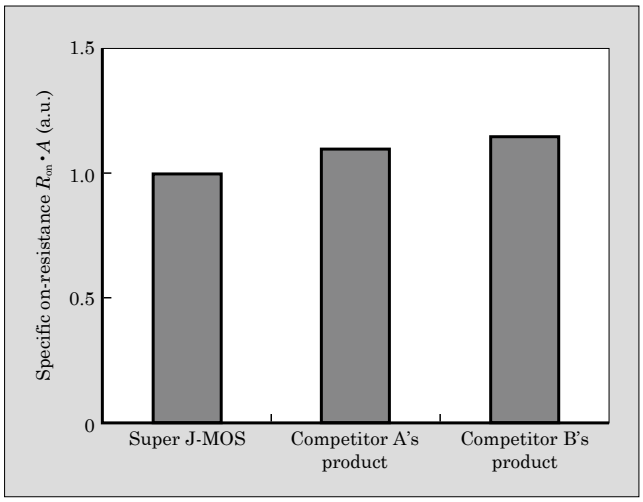

Fig.4 Comparison and evaluation of R_{on}・A

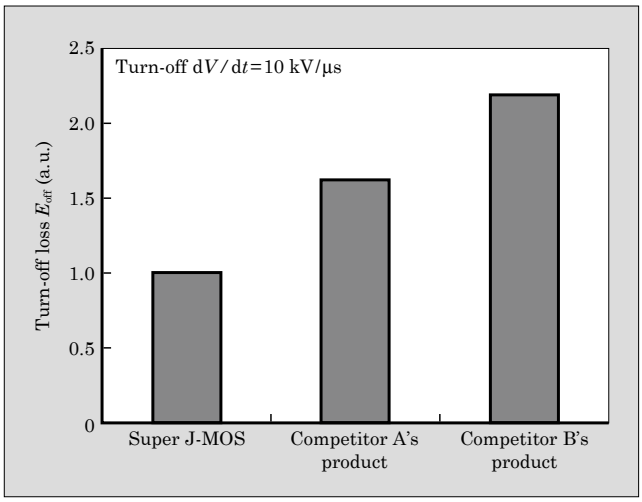

Fig.5 Comparison and evaluation of E_{off}

tionship between E_{off} and turn-off dV/dt was improved.

4. Super J-MOS Performance

4.1 Evaluation of on-resistance

For SJ-MOSFETs rated at 600 V/20 A/0.19 Ω, the specific on-resistances R_{on}・A at rated voltages of the Super J-MOS and competitors' products were compared and evaluated. Figure 4 shows the evaluation results. The values of R_{on}・A are relative to the value of the Super J-MOS. With the Super J-MOS, R_{on}・A values equal to or better than those of competitors' SJ-MOSFETs were confirmed.

4.2 Evaluation of switching loss

Next, E_{off} was evaluated. With the Super J-MOS, the E_{off} value is 160 μJ when turn-off dV/dt is 10 kV/μs, and this extremely small E_{off} was realized through structural optimization. E_{off} values when turn-off dV/dt is 10 kV/μs were compared and evaluated for the Super J-MOS and competitors' products, and the results are shown in Fig. 5. As in the case of Fig. 4, E_{off} values are relative to the value of the Super J-MOS.

As shown in Fig. 5, the Super J-MOS is affected by the structural optimization and the results showed an E_{off} value significantly lower than those of competitors' products.

5. Investigation in Electrical Equipment

As described above, by optimizing the surface structures, the Super J-MOS was confirmed to exhibit excellent levels of R_{on}・A and E_{off}. Next, to verify the power efficiency when using a Super J-MOS, a Super J-MOS was installed in the power factor correction (PFC) circuit of a 400 W-ATX power supply as shown in Fig. 6, and the power efficiency was evaluated. The same evaluation was also performed for company A's SJ-MOSFET, which exhibited lowest turn-off loss

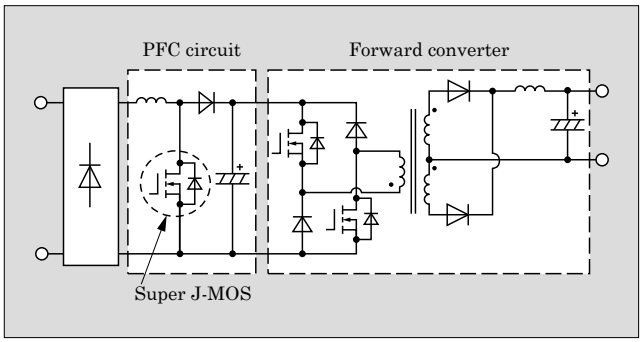

Fig.6 Configuration of PFC circuit

among the competitors' products. The values of power supply loss and power supply efficiency that were obtained were compared and evaluated (see Fig. 7). All the devices that were evaluated were rated at 600 V/0.19 Ω.

As shown in Fig. 7(a), in comparison to company A's product, the Super J-MOS exhibits lower loss especially during turn-off, and this contributes greatly to a reduction in total power supply loss.

Moreover, as shown in Fig. 7(b), highly efficient power supply operation is realized with the Super J-MOS, and when the power supply has a 50% load factor, the power efficiency is at the high level of 96%. Furthermore, in the load factor range from 20% to 100%, the power efficiency was at least 94% or higher. This result conforms to the "80 PLUS[6] "*2 standard, and indicates that the Super J-MOS possess characteristics that can contribute to improvement of the power

*2: "80 PLUS" : A standard promoting higher efficiency in power supplies and is defined by an independent private organization (http://www.80plus.org). In the power supplies used in PC and servers, 80 PLUS certification indicates that the power conversion efficiency is 80% or greater at load factors of 20%, 50% and 100%.
80 PLUS is a trademark or registered trademark of US-based Ecos Consulting Inc.

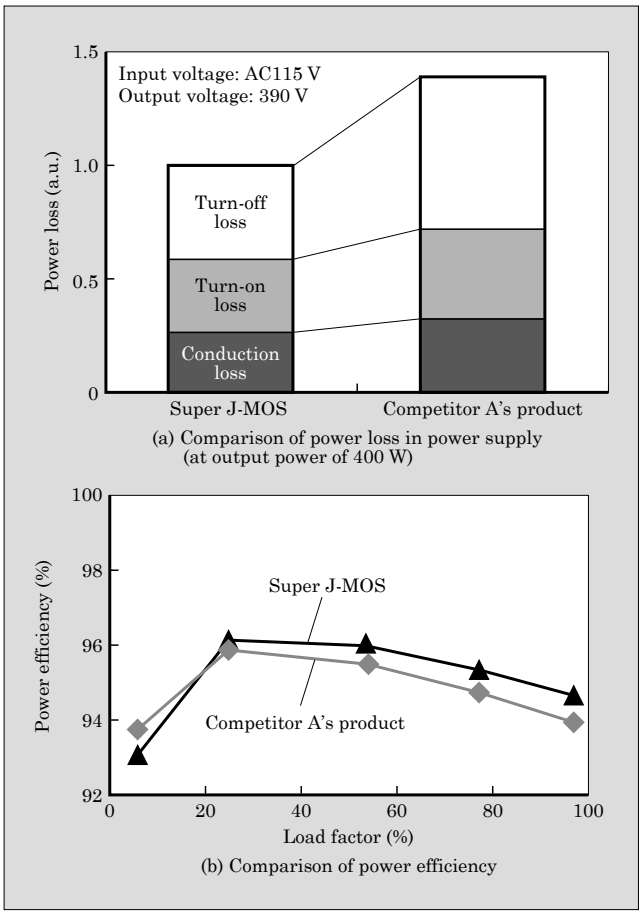

Fig.7 Results of investigation in electric equipment

efficiency of a power converter.

6. Postscript

By optimizing the surface structures of the SJ-MOSFET, the "Super J-MOS," which features an improved tradeoff relationship between turn-off loss and turn-off dV/dt and low switching loss, was developed. Increasing the gate-to-drain capacitance and lowering the threshold voltage was confirmed to result in a lower turn-off dV/dt and an improved tradeoff relationship between turn-off loss and turn-off dV/dt. By optimizing the surface structures of the device, the turn-off loss was found to be 160 μJ when turn-off dV/dt is 10 kV/μs, and this is an excellent level for a SJ-MOSFET. Additionally, as a result of installing a Super J-MOS in the PFC circuit of a 400 W-ATX power supply and then conducting an evaluation, power supply operation exhibiting much higher efficiency than that of competitors' SJ-MOSFETs was found to be possible.

Targeting applications in the communication and PC server power supply market, Fuji Electric is currently moving forward with efforts to reduce loss and increase the efficiency of the 600 V-rated Super J-MOS. Fuji Electric intends to continue to improve device performance in the future through device miniaturization and the like.

References

(1) Fujihira, T. "Theory of Semiconductor Superjunction Devices," Jpn. J. Appl. Phys., 1997, vol.36, p.6254-6262.

(2) Deboy, G. et al. "A New Generation of High Voltage MOSFETs Breaks the Limit Line of Silicon," Proc. IEDM, 1998, p.683-685.

(3) Onishi, Y. et al. "24 mΩcm² 680 V Silicon Superjunction MOSFET," Proc. ISPSD' 02, 2002, p.241-244.

(4) Saito, W. et al. "A 15.5 mΩcm²-680 V Superjunction MOSFET Reduced On-Resistance by Lateral Pitch Narrowing," Proc. ISPSD' 06, 2006, p.293-296.

(5) Baliga, B. J. Modern Power Devices, John Wiley & Sons, Inc., 1987, p.305-314.

(6) ECOS Consulting. http://www.80plus.org. (Refer to Jul. 29, 2011)