UDC 621.316.7

FUJI PROGRAMMABLE CONTROLLER "FUJILOG-μH"

Tokutaro Shimbo
Yoh Kikuchi
Kohji Koizumi
Kazuhiro Fujita
Masakatsu Hishinuma

I. INTRODUCTION

Programmable controllers (hereinafter abbreviated to as PC) appeared in the market for taking place of relay control panels have been rapidly and greatly developed in response to the developments of micro processors and semiconductor memories.

One of the developments is seen in the highly graded operating functions called a highly functional PC. Adding digital control operating functions which perform various operations in the unit of a byte or word to the sequence control operating functions the main purpose of which is a bit logic operation, this controller can be applied to the control fields which cannot be covered by the conventional relay controllers.

FUJILOG-μH introduced in this paper is aiming at the above purpose. Following the controllability bit processing function of the already existing FUJILOG-μT, the instruction system is expanded so that sequence controls can be programmed efficiently including small scale digital controls. Further, the PC allows the program memory capacity and processing speed to increase, and it is fulfilled with RAS functions.

Moreover, this PC is so designed that various system interfaces can be added easily. Therefore, this PC can be used not only by installing it alone but also hierarchy or decentralized system can be composed. This PC features the wide application range. The outline follows.

II. SYSTEM CONFIGURATION

This PC consists of a central processing unit, input/output unit, input/out card and auxiliary power supply. *Figs. 1* and *2* show the appearance and system configuration respectively.

The central processing unit consists of a control power supply which operates the system, program memory into which the control operation programs are stored, arithmetic unit which executes the programs, I/O units and interface units with the programming equipment. The printed circuit boards divided by each functional circuit are accommodated in a rack.

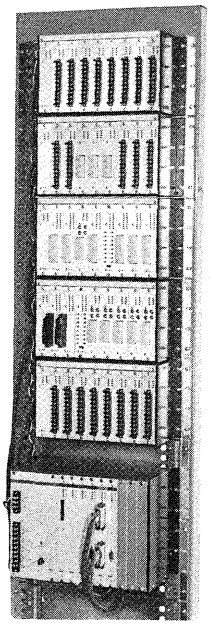

Fig. 1 Appearance of FUJILOG-μH

The I/O units function as interfaces between the PC and process machines, and consists of the input/output interface cards which send and receive signals to and from the central processing unit, and the rack into which the cards are accommodated. This rack is capable of accommodating maximum of eight I/O cards which send and receive signals to and from external input/output machines and equipment. For the applicable input/output cards, UT5000/UT6000 series input/output cards which are equipped with input or output circuits of eight points per card are available. In addition to these cards, UT1600 series input/output card equipped with input or output circuit of 16 points has been developed, improving equipment density. With the availability of various input/output cards, when an eight point I/O card is installed, maximum 64 points or when a 16 point I/O card is installed, maximum 128 points of input/output can be used per I/O unit. No eight point card and 16 point card can be mixed within a unit, but they can be mixed in the unit of an I/O unit. In

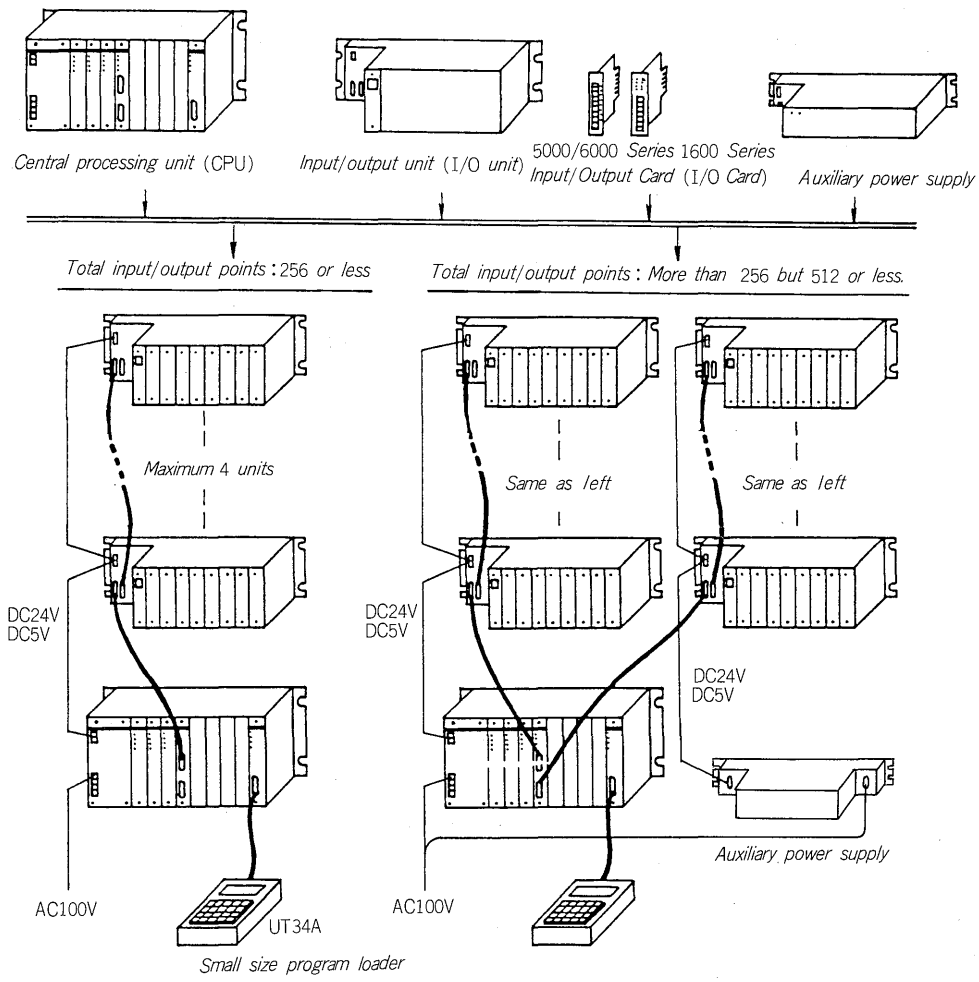

Fig. 2 System configuration of FUJILOG-μH

this case, input/output address range occupied by the unit differs depending on a type of the installed I/O card. However, this address space can be set in 64 point boundary by dip switch within the I/O interface card (LIOC), allowing a mixed use of different types of card.

The auxiliary power supply replenishes capacity of the central processing unit control power supply. In case of a system the number input/output points of which exceeds 256, the central processing unit control power supply takes care of the 256 points, and the auxiliary power supply takes care of the input/output points exceeding the 256 points. Accordingly, the input voltage for the auxiliary power supply must be controlled simultaneously with that to the central processing unit.

The central processing unit and I/O unit, one I/O unit and other I/O unit, and auxiliary power supply and I/O units are joined with the individual signal and control power supply cables.

III. SPECIFICATIONS AND FUNCTIONS

1. Specifications

1) Specifications of central processing unit

Table 1 shows the specifications of the central processing unit.

The input/output transfer system of this PC is of an overall transfer type, and the program execution is a cyclic operation type which excecutes programs repeatedly from zero step of the program memory to the END instruction storing step. Accordingly, the cycle time varies successively depending on the number of executed instructions and type. As shown in the Table 1, a standard cycle time is set, and when loading a program, the standard time is arithmetically obtained based on the program content, and the cycle time is automatically fixed at the standard execution time. The fixed cycle time can be read out and checked by the program loader.

For this PC starting mode, there are automatic mode and manual mode. Under the automatic starting mode, the PC starts operating automatically when power is supplied. Under the manual mode, the PC does not start even if power is supplied and it starts operating in accordance with start instruction.

For operation mode, there are RUN mode which is a normal operation mode and TEST mode which is for program debugging. Table 2 shows the differences between RUN and TEST modes.

Table 1 Central processing unit specifications of FUJILOG-μH

Item			Specification
Control/ operation unit	Control system		Cyclic operation
	Program system		Stored program
	Control/operating function		• Sequence control operation AND, OR, Flip flop, Timer, Counter, Shiftregister, Step controller, Rising/Lowering detection • Sequence control extended operation Data transfer, Comparison, Numeric operation(+.–), Data operation (Logic, Inversion, Shift, Addition/Subtraction)
	Type of instruction		Sequence control instruction: 25 types Sequence control extending instruction: 25 types Program control instruction and others: 5 types
	Operating speed	One instruction processing time	Sequence control instruction: 1.5 to 2.3 μs/instruction Sequence control extending instruction: 5 to 8.2 μs/instruction
		Cycle time	10, 16.7, 20, 25, 33.3 ms (Variable depending on type of instruction and program length, In case of a sequence control instruction and 8k step, cycle time is 25 ms.)
	Data memory	Capacity	1024 bytes Including input/output buffer, data operating register and flag register
		Use segment	For sequence control: 4096 points (512 bytes); for input/output buffer, auxiliary relay, timer, counter, shift register and step controller For sequence control extension: 1024 bytes (512 bytes are used commonly with the sequence control); Power failure holding area can be designated.
Program memory unit	Type of memory		CMOS RAM (Battery back up) EP-ROM (Option)
	Capacity. Unit of additional installation		CMOS RAM: Expansion can be made in the unit of 8k words, 2k words EP-ROM: Fixed in 8k words
Input/ output control unit	Maximum number of input/output control points		1024 points (Simultaneous control can be made in the unit of 8 points)
	Number of applicable input/ output units		Maximum 8 units/LIOC
Power supply unit	Input voltage-Fluctuation range		AC100V, –15~+10% 50/60Hz
	Capacity		380VA
	Input/output control capacity		For 256 points
Self-diagnosis			Checking operation, battery, memory, program and input/output etc.
			Displays state of normal/abnormal in the unit of a module
Control-alarm input/output			Normal operation output: STX1 Abnormal output: STX2, 3, 4 (Type of abnormal), ALM1, 2 (Abnormal level) Start mode switch: AUTO/MANU Operation mode switch: RUN/TEST Start·Stop switch: START, STOP System reset switch: RESET
General specifications	Ambient temperature		0~45°C
	Ambient humidity		10~85% RH (Without condensation)
	Vibration		0.8G
	Noise resistance		Noise simulator 1 000V
	Dielectric strength		AC 1500V 1 minute
External dimensions (mm)			400(W) x 262(H) x 195(D)

Table 2 Function of RUN/TEST mode of FUJILOG-μH

Item \ Operation mode	RUN	TEST
Scan time	Variable (10, 16.7, 20, 25, 33.3 ms)	Fixed (100 ms)
Output under the stop mode	Reset	Hold (successive output)
STOP → START	Initialize	Sucessive start
RUN indicating lamp	Flicker of about 200 ms cycle	Flicker of about 800 ms cycle

The RUN indicator lamp flickers in about 400 ms cycle when several seconds are elapsed after supplying power for about 15 seconds. During this period, no processing is made.

Table 3 Various alarming functions of FUJILOG-μH

Item	STX	ALM	Content	Actions to be taken
Normal	1	–	Normal operation	–
Internal fault	2	1	Fault of card, module, internal bus, etc.	Stop, output reset
		2	Fault of LDIF	Operation continues
Battery fault	3	1	No battery after supplying power, dropped battery voltage, etc. are detected.	Stop, output reset
		2	Fault in the battery system other than those immediately after connecting the battery is detected.	Operation continues

Table 4 Various alarm indicators of FUJILOG-μH

RUN	A 1	A 2	A 3	CPU	ALU	MEM	LIOC	LDIF
●	○	○	○	Normal: ON	Normal: ON	Normal: ON	Normal: ON	Normal: ON
○	●	○	○	Other device fault (ALU, LDIF, LIOC etc.)		Dropped battery voltage 1 error	I/O bus fault	
○	○	●	○	Clock pulse fault	Overtime error	Dropped battery voltage 2 error	I/O rack power fault	
○	●	●	○	LIOC data memory access domain duplicate		Disconnected battery cable	I/O composing data error	
○	○	○	●	Read error	Read error	Interrupting generator fault	Read error	Read error
○	●	○	●	Main memory RAM fault	Undefined instruction check	Program memory content error	Main memory RAM fault	Main memory RAM fault
○	○	●	●	RAM fault	DSR logic fault	Battery supervisory circuit fault	RAM fault	RAM fault
○	●	●	●	PROM fault Program over run	Control circuit fault	Memory not ready	PROM error, data memory inhibit domain set	PROM fault
●	●	●	●	Other device fault (Power supply unit)				

●	○	○	○	Level "0" Bus error (Spare)
●	○	○	●	Level "1" Bus error (Spare)
●	○	●	○	Level "2" Bus error (Spare)
●	○	●	●	Level "3" Bus error (CPU error)
●	●	○	○	Level "4" Bus error (LDIF error)
●	●	○	●	Level "5" Bus error (LIOC error)
●	●	●	○	Level "6" Bus error (Spare)
●	●	●	●	Level "7" Bus error (ALU error)

Table 5 I/O unit specifications of FUJILOG-μH

Item	Specifications
Maximum number of installed I/O points	64 points at an 8 point unit card 128 points at a 16 point unit card
Applicable I/O card	8 point card: 5000/6000 series 16 point card: 1600 series
Control power supply	Supplied from central processing unit or auxiliary power supply
I/O card installing method	I/O card free location installing method
External dimensions (mm)	400(W) x 200(H) x 185(D)

Table 6 I/O unit number and address of FUJILOG-μH

I/O unit number	Card number range	I/O relay number range
0	0~ 7	0.0~ 7.7
1	8~15	8.0~15.7
2	16~23	16.0~23.7
3	24~31	24.0~31.7
4	32~39	32.0~39.7
5	40~47	40.0~47.7
6	48~55	48.0~55.7
7	56~63	56.0~63.7

The PC can be started, operating mode can be selected and operating and stopping instructions can be sent from the control/display panel on the face of the central processing unit.

This PC has various self-diagnostic functions, and in response to the content of each abnormal condition, alarm and display are made.

Alarming is output with STX1-3 contacts which indicate type of abnormal occurrence and ALM1 and 2 contacts which indicate abnromal level. *Table 3* shows these contact operating conditions when abnormal occurrences are detected.

For fault indication, type of abnormal occurrence within that circuit is indicated in the unit of each functional circuit, the common bus is checked with CPU card, and thus, bus error is also displayed. *Table 4* shows the correspondence between the error display pattern and cause of the error.

2) Specifications of input/output unit

Table 5 shows specifications of the input/output unit.

The input/output address range occupied by the input/output unit corresponds to the input/output unit numbers set by the two sets of dip switch in the input/output inter-

Table 7 Input/output card specifications of FUJILOG-μH

Kind		Type	Voltage	Current	Remarks
Input	8-point card	UT5220/6220, 6221	DC24V	typ. 10 mA	
		UT5140/6140, 6141	AC100V	typ. 10 mA	
		UT5150/6150, 6151	AC200V	typ. 10 mA	
	16-point card	UT1631*	DC24V	typ. 10 mA	
		UT1621*	AC100V	typ. 10 mA	
Output	8-point card	UT5422	DC24V	1 mA~2A	Transistor output
		UT6420/6422	DC24/48V		
		UT5342	AC100V	10 mA~2A	Triac output
		UT5352	AC200V	10 mA~2A	
		UT6331/6332	AC100~200V	10 mA~1/2A	
		UT5502/6502, 6503	AC·DC220V	10 mA~2A	Relay contact output
		UT6522			
	16-point card	UT1611*	DC24~48V	0.5A	Transistor output
		UT1601*	AC100~200V	0.5A	Triac output
Others		UT1651*	DC24V	10 mA input, 0.15A output	Input/output mixed card
		UT5702	–	–	Dummy (display only)
		UT5701A/UT6701	–/AC100~200V	–/10 mA~2A	Latch/latch contact output
		UT5703/UT1693*	–	–	Test input
		UT6710	–	–	BCD 5 digit counter
		TU6711	–	–	4 kHz

NOTE) *denotes I/O cards for FUJILOG-μH only, and others are used commonly with FUJILOG-μT.

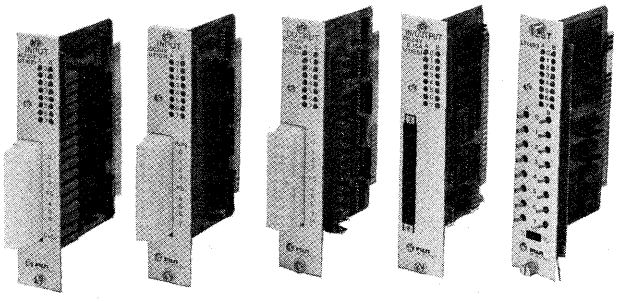

Fig. 3 Appearances of I/O cards of FUJILOG-μH

face card as shown in *Table 6*. One set of the dip switch consists of 3 bits for setting unit number and one bit for enable signal (total 4 bits). When an eight point input/output card is installed, one set of dip switch is installed and when a 16 point input/output card is installed, two sets of dip switch are installed separately.

The card addresses within an input/output unit are fixed. The input/output card can be installed freely in any desired position, and one card address or successive two card addresses are allocated to the installed input/output cards respectively for an 8 point or 16 point input/output card.

3) Specifications of Input/Output card

Table 7 shows the outline of the input/output cards used for this PC, and *Fig. 3* shows the appearances.

The input/output cards of UT5000 and UT6000 series are used commonly with FUJILOG-μT which is smaller than the FUJILOG-μH, and input/output cards of UT1600 series are for this PC only.

4)

Table 8 shows the specifications of the auxiliary power supply unit.

Table 8 Specifications of auxiliary power supply unit of FUJILOG-μH

Item	Specifications
Input voltage · Fluctuation range	AC100V –15~+10% 50/60 Hz
Capacity	270VA
Output voltage	+5V, +24V
Input/output control capacity	For 256 points
External dimensions (mm)	400(W), 100(H), 95(D)

2. Functions

1) Configuration and function of central processing unit

Fig. 4 shows the fundamental configuration of the central processing unit.

The card units such as CPU, MEM, ALU, LIOC and LDIF are composed based on the micro processor except for the MEM, and coupling these units with a common bus, a multi-processor system is composed. This architecture eases expansion of function, decentralizes the control functions, improves the processing time and allows a precise self-diagnosing.

The CPU card performs macro-coordination for the internal processing of the PC, common bus management for

data transfer between cards by DMA system which is made through the common bus and data transfer control.

In the MEM card, user's application programs are stored.

The ALU card executes application programs and controls input and output of the PC. In this card, the arithmetic operation circuit as shown in *Fig. 5* is realized by combining logic IC and micro processor around the ARG register into which bit operation results are stored and BRG register into which byte operation resutls controlled by the contents of the ARG register are stored.

The LIOC transfers the input/output control signals obtained based on the execution results of the ALU to the input/output unit, and controls the input/output unit. To the LIOC, two external input/output buses can be connected, and with one external input/output bus, maximum four input/output units can be coupled.

The LDIF is an interface unit with the programming devices, and through this card, signals are sent and received to and from the programming devices.

2) Configuration and function of card unit

The configuration of each card unit which composes the central processing unit is approximately same except for the MEM. *Fig. 6* shows the standard configuration.

Into the PROM, system programs are stored, and RAM is used to store data temporarily when executing the CPU within the card.

Within the card, data are transferred through the on-board-bus.

3) Configuration and function of input/output unit

Fig. 7 shows the fundamental configuration of the input/output unit.

The input/output interface unit is connected with the external bus. This unit selects input/output control signal within the input/output address range which corresponds to its own unit number, and controls the input/output cards on the unit.

IV. PROGRAMMING

The instruction structure that describes control opera-

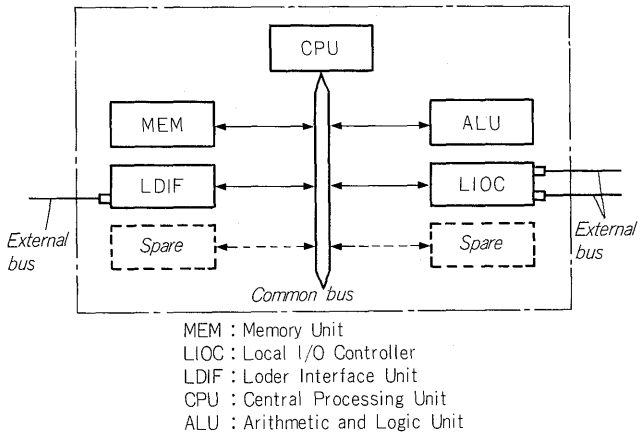

Fig. 4 Fundamental configuration of central processing unit of FUJILOG-μH

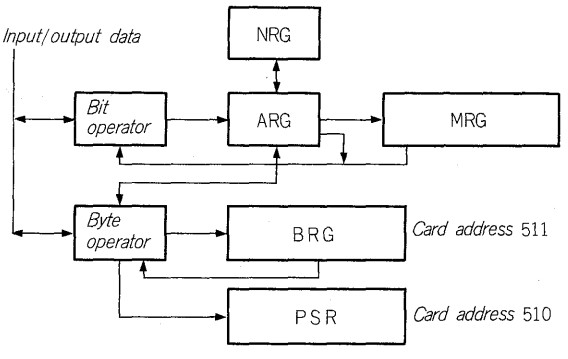

Fig. 5 Arithmetic and logic unit configuration of FUJILOG-μH

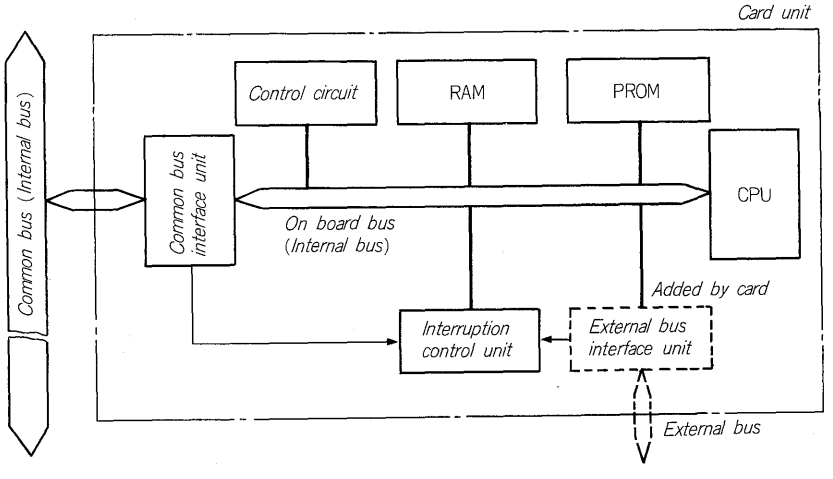

Fig. 6 Standard device configuration of FUJILOG-μH

Table 9 Instruction structure for FUJILOG-μH

Sequence control instruction			
Function	Name	Symbol	Operation
Input/output	READ	R	Power supply connection
	READ NOT	RN	Contact b power supply connection
	WRITE	W	Output
Logic arithmetic processing	AND	A	Series connection
	AND NOT	AN	Contact b series
	OR	O	Parallel connection
	OR NOT	ON	Contact b parallel connection
	AND MRG	A MRG	Intermediate memory series connection
	AND NOT MRG	AN MRG	Intermediate memory contact b series connection
	OR MRG	O MRG	Intermediate memory parallel connection
	OR NOT MRG	ON MRG	Intermediate memory contact b parallel connection
Flip flop	SET	S*	Set
	SET NOT	SN*	Reset
	DIFFERENTIAL	D*	Rising differential
	DIFFERENTIAL NOT	DN*	Lowering differential
Functional arithmetic processing	DATA SET	DS	Data direct set
	DATA SET FROM CARD	DC*	Data indirect set
	WRITE TIMER	W TMR	0.1 second clock timer
	WRITE IS BASE TIMER	W T1*	1 second clock timer
	WRITE LOS BASE TIMER	W T10*	10 second clock timer
	WRITE COUNTER	W CTR	Counter
	WRITE SHIFT REGISTER	W SR	Shist register
	WRITE STEP CONTROLLER	W SC	Step controller
Common interlock	WRITE NRG	W NRG	Master control set
	WRITE NOT MRG	WN NRG	Master control reset
Skip	JUMP START	JS*	Skip start
	JUMP END	JE*	Skip end
Others	END	END*	Program end
	CLEAR	CLR	Card clear
	NO OPERATION	NOP	Non execution

Sequence control expanded instruction			
Function	EM No.	Symbol	Operation
Transfer	EM 0	LD	Load (CARD) to (BRG)
	EM 1	LDI	Load immediate to (BRG)
	EM 2	ST	Store (CARD) from (BRG)
Addition	EM 10	ADD	Add (CARD) to (BRG)
	EM 11	ADDI	Add immediate to (BRG)
	EM 12	ADC	Add (CARD) to (BRG) with carry
	EM 13	ADCI	Add immediate to (BRG) with carry
Subtraction	EM 14	SUB	Subtract (CARD) from (BRG)
	EM 15	SUBI	Subtract immediate from (BRG)
	EM 16	SBB	Subtract (CARD) from (BRG) with borrow
	EM 17	SBBI	Subtract immediate from (BRG) with borrow
Comparison	EM 18	CP	Compare (CARD) with (BRG)
	EM 19	CPI	Compare immediate with (BRG)
Logic	EM 20	AND	And (CARD) with (BRG)
	EM 21	ANDI	And immediate with (BRG)
	EM 22	OR	Or (CARD) with (BRG)
	EM 23	ORI	Or immediate with (BRG)
Inversion	EM 24	INV	Invert
	EM 25	NEG	Negative
Increment/Decrement	EM 26	INC	Increment (BRG)
	EM 27	DEC	Decrement (BRG)
Shift	EM 28	SRC	Shift right circular (BRG)
	EM 29	SLC	Shift left circular (BRG)
	EM 30	SRCC	Shift right circular (BRG) with carry
	EM 31	SLCC	Shift left circular (BRG) with carry

Note
(1) Those instructions accompanied with asterisk (*) are newly set up for FUJILOG-μH. Others are in the same source level as FUJILOG-μT.
(2) All of these are newly set for FUJILOG-μH.

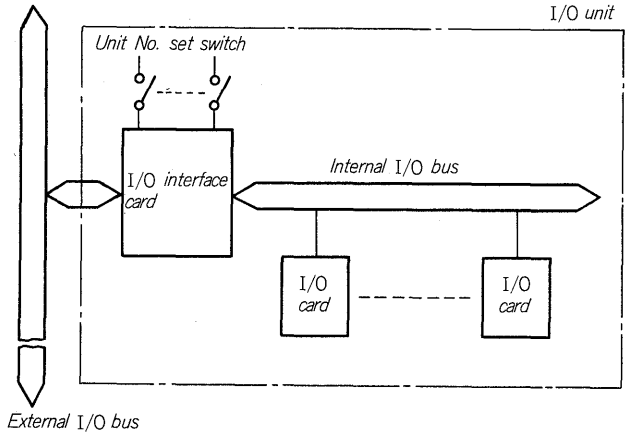

Fig. 7 Fundamental configuration of input/output unit of FUJILOG-μH

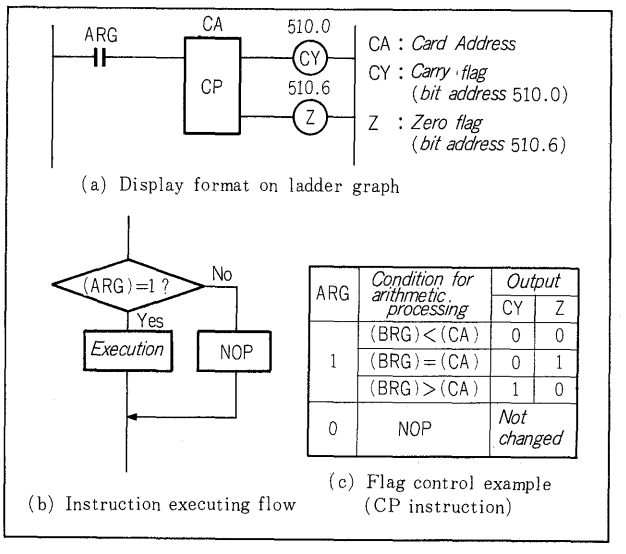

Fig. 8 Sequence control expanded instruction executing format for FUJIOG-μH

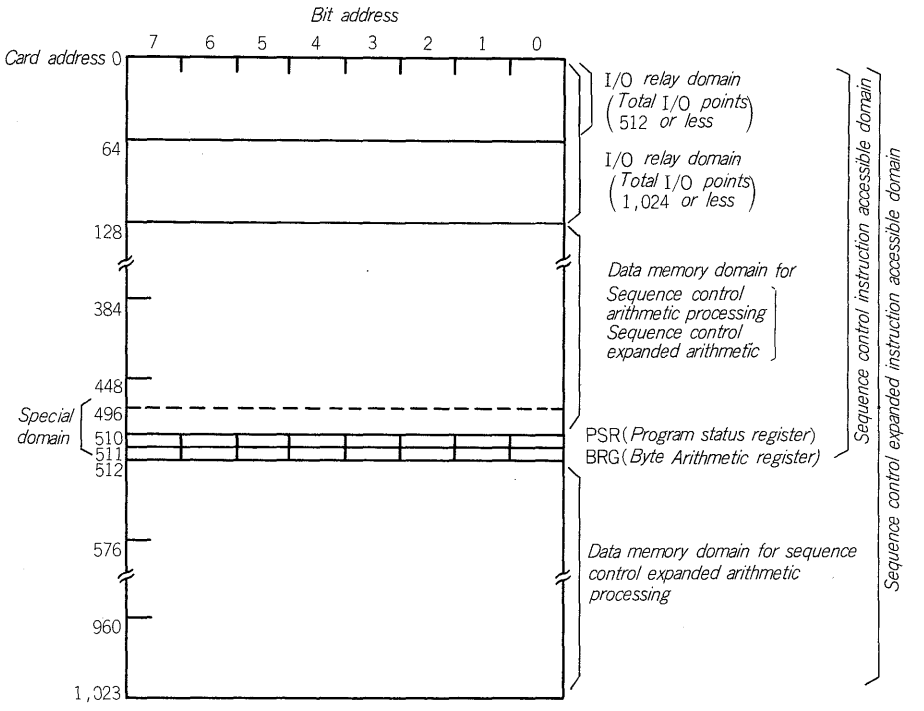

Fig. 9 Data memory map of FUJILOG-μH

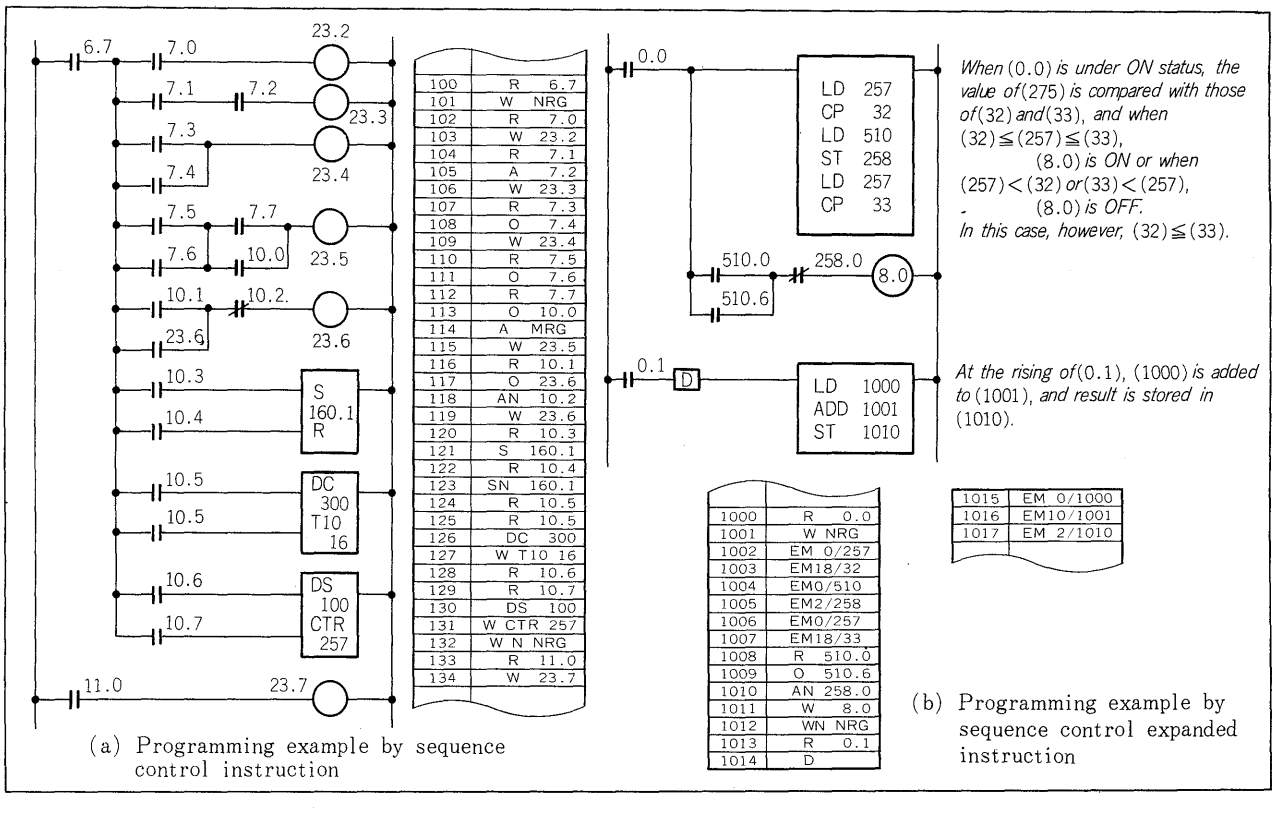

Fig. 10 Programming example of FUJILOG-μH

tions of this PC are based on the programs from the expression of the operations to be controlled by the relay ladder diagram.

For the used instructions, there are sequence instructions and sequence control expanded instructions. The sequence control instructions are mainly for bit arithmetic processing. The sequence control expanded instructions are mainly for byte arithmetic processing for digital control programs, which is comparatively simple and executed by combining with the sequence control.

The sequence control instructions includes the instruction structure of the FUJILOG-μT which is smaller than this PC.

Types of the instructions are shown in *Table 9*.

For the sequence expanded instructions, such a format as that executions of the instructions can be controlled by contact signal conditions (contents of ARG) as shown in *Fig. 8* is used so that the combinations with the sequence control can be described efficiently.

There are 1024 bytes of data memory. *Fig. 9* shows the data memory map.

Bit access can be made for 512 bytes (0 to 511) of the card address, and these addresses can be designated by the sequence control instructions. In this domain, however, input/output buffer domain and special domains including PSR and BRG registers which store execution results and status flags at the time of execution of sequence control expanded instruction exist, and in this special domain, writing by program is inhibited.

All the 1024 bytes of card addresses 0 to 1023 can be designated by sequence control expanded instructions. However, for the special domain, reading can be made in the unit of a byte only as well as the sequence control instructions.

For the non-volatile data memory, any desired eight blocks can be designated by program loader. To be more specific, any desired data memory card address section may be written into eight non-volatile domain set registers, and for all range from 0 to 1023, one register can be designated.

It is also possible to preset various data used by the program on the data memory from the program loader.

V. PROGRAMMING EXAMPLE

Fig. 10 (a) shows programming example by the use of sequence contol instruction. In this figure, when contacts 6 and 7 are OFF, output 23.6 is OFF, however, 160.1 holds the previous status. Moreover, the contents of timer 16 and counter 257 are reset.

Since the set value of the timer 16 is designated by card address 300 of the data memory it is necessary to set the data in advance.

Fig. 10 (b) shows programming example by the use of sequence control expanded instructions.

With this instruction, arithmetic operations are made between the content of BRG and data designated by the program.

When executing a CP instruction, the contents of the program status register change, and for this reason, flag status is saved in card 258 when executing step 1,003 at steps 1004 and 1005.

VI. POSTSCRIPT

The application range of the PC to which digital control functions are added will be expanded in the intermediate control field between relay control and computer control by changing the concept of the conventional control system configuration.

This PC has the flexibility in composing the system which is capable of accepting various requirements requested when the application range is expanded as described above. The functions of this PC will be increased further in response to the needs for the applications.

TOPICS

TAIPEI INTERNATIONAL AUTOMATION EQUIPMENT EXHIBITION OPENED

EXPORT–ASIA DEPARTMENT STANDARD PRODUCT GROUP

Fuji Electric participated in the International Automation Equipment Exhibition held at the Taipei International Trade Center.

The exhibition was held in response to the industrial automation, rationalization and improved product quality policy of the government of Taiwan and the demand of the business community.

Held from March 19 to 24, the exhibition attracted the attention of the associated industries and was attended by 130,000 people.

Fuji Electric displayed its seeing-eye robot, programmable controller, variable speed motor incorporating the newest technology. The display stressed the point that it can meet a wide range of demands in all fields up to drive, control, and detection and even systems.

In the future, Fuji Electric intends to establish an export organization to contribute to the promotion of rationalization around the world.