2nd-Generation Discrete SiC-SBD 1,200-V Series

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In recent years, the increase in worldwide data traffic has accelerated the installation of data centers and telecommunication base stations. Since data centers require a stable supply of power, they use uninterruptible power systems (UPSs). The power semiconductors used in UPSs are requiring lower loss and higher durability.

Fuji Electric has developed the 2nd-generation discrete SiC-SBD 1,200-V Series as a line-up that achieves lower loss by reducing forward voltage V_F and improves surge forward current I_{FSM} compared with the 1st-generation discrete SiC-SBD Series.(1)

1. Features

Figure 1 shows the package appearance of the 2nd-generation discrete SiC-SBD 1,200-V Series, and Table 1 provides an overview of the product line-up. The main features are as follows.

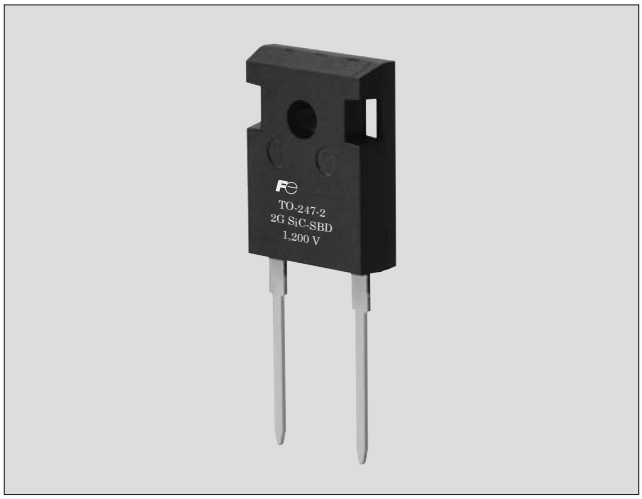

Fig.1 Package appearance

(a) Its low forward voltage (T_{vj} = 25°C, 10% lower than conventional products) contributes to improved efficiency in applicable power supply equipment.
(b) Improved I_{FSM} (surge forward current) (T_{vj} = 25°C, 110% better than conventional models) improves dielectric strength against large instantaneous forward currents (inrush currents).

2. Chip Technology

SIC-SBDs exhibit small switching loss during reverse recovery operation since they are unipolar majority carrier devices that contribute to conduction without any accumulation effect. This mean that in order to reduce device loss, it is necessary to reduce conduction loss by decreasing V_F. In addition, diodes in a power factor correction (PFC) circuit must not be damaged by the inrush current when smoothing capacitors charge at the power supply turned on.

Figure 2 shows the structure of the 1st- and 2nd-

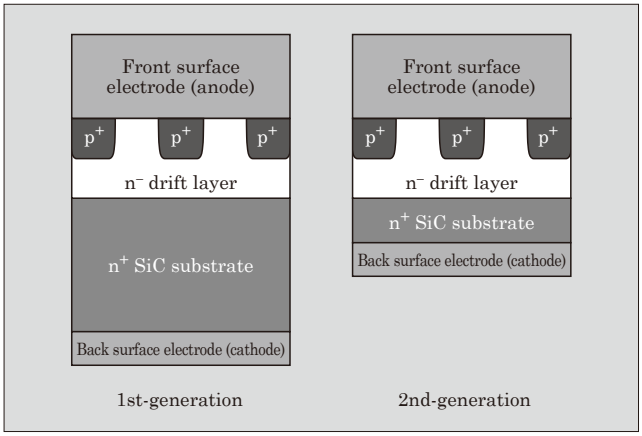

Fig.2 Structure of the 1st- and 2nd-generation SiC-SBD chips

Table 1 Line-up

Type	Package	Maximum ratings			Electrical characteristic	
		V_{RRM}	I_F	I_{FSM}	V_F T_{vj} = 25°C (typ.)	V_F T_{vj} = 150°C (typ.)
		(V)	(A)	(A)	(V)	(V)
FDC2 WT20S120	TO-247-2	1,200	20	190	1.57	2.29
FDC2 WT40S120	TO-247-2	1,200	20	305	1.57	2.29

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generation SiC-SBD chips. Both utilize junction barrier Schottky (JBS) structures with a p^+ layer on their device surface. We have reduced n^+ SiC substrate thickness, reduced barrier height by optimizing the Schottky junction, reduced drift resistance by optimizing the JBS structure and drift layer, and reducing contact resistance by using proprietary wafer process technology, allowing the 2nd-generation SiC-SBD to have reduced V_F and improved I_{FSM}.

Figure 3 shows the temperature characteristics of V_F for 1st- and 2nd-generation products with a 1,200 V/20 A rating when I_F = 20 A. For the entire region between −55°C and +125°C, 2nd-generation products have lower V_F, and when T_{vj} = 25°C, V_F is 10% lower than 1st-generation products.

Figure 4 shows the I_F–V_F characteristics of a 1,200-V/20-A device in the high current range. When the pn junction diode consisting of the p^+ and n^- drift layers in contact with the surface electrode (anode) operates, a large current of 100 A or more flows through

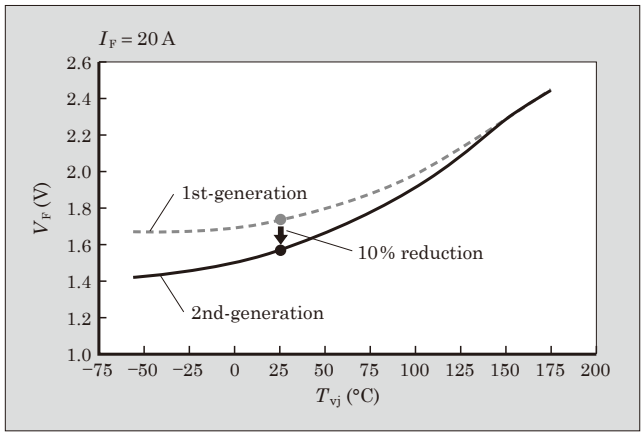

Fig.3 V_F temperature characteristics of 1st- and 2nd-generation 1,200-V, 20-A devices

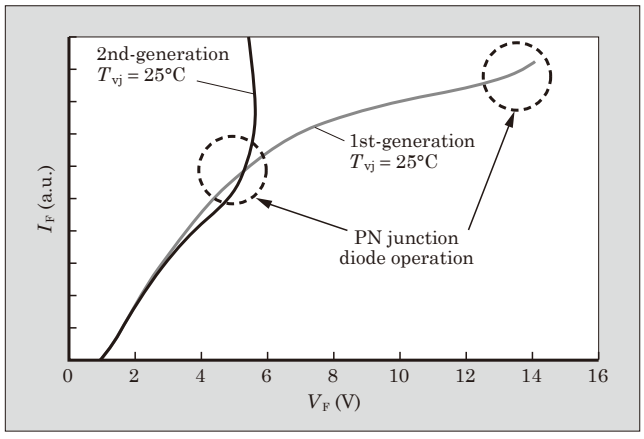

Fig.4 I_F – V_F characteristics in the high-current range of 1st- and 2nd-generation 1,200-V, 20-A devices

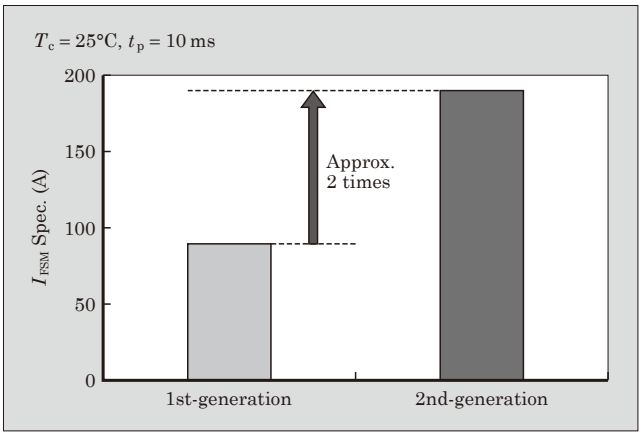

Fig.5 I_{FSM} characteristics of 1st- and 2nd-generation 1,200-V, 20-A devices

the ohmic region of the surface electrode (anode) and the p^+ layer. The 2nd-generation device has an optimized JBS structure that allows current to flow through the pn junction diode more easily than the 1st-generation products. As shown in Fig. 5, the guaranteed I_{FSM} value has been increased twice, 190 A for the 2nd-generation products than 90 A for the 2nd-generation products, due to thermal resistance reduction (improved heat dissipation) through thinner n^+ SiC substrate.

3. Package

This device uses the TO-247-2 package, presenting an industry standard TO-247 outward form, which has two terminals with no center terminal. Since the creepage distance (insulation distance) between terminals is longer than that of 3-terminal products, its insulation performance is higher, and its structure is suitable for applications that need a high dielectric strength. In addition, using lead-free solder for the connections between the chip and lead frame is compliant with the RoHS Directive (EU 2011/65/EC).

References

(1) Watanabe, S. et al. 2nd-Generation Discrete SiC-SBD Series. FUJI ELECTRIC REVIEW. 2021, vol.67, no.4, p.263-267.

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