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FUJI PROGRAMMABLE CONTROLLER "FUJILOG-μT" SERIES

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I. FOREWARD

Based on the accumulation of control technologies over many years, we have offered two programmable controllers (PC), the F-MATIC SC Series and FUJILOG Series, to meet a broad range of demands. We have now commercialized and added the FUJILOG-μT Series to meet the trend in the market. This new series will be outlined here.

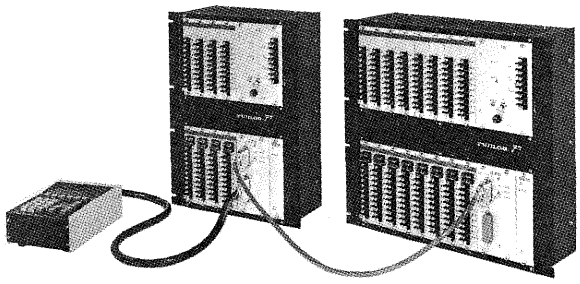


Fig. 1 Exterior view of FUJILOG-μT

II. FEATURES

The FUJILOG-μT has been developed to replace the control relay panel in the medium and small scale control fields and numerous considerations have been given from not only the standpoint of price, but also from the standpoints of functions and handling.

(1) Instruction words consists of four basic instructions, numerous functional instructions, and a decimal numbers address. Moreover, since they consist of an easy-to-understand ladder diagram which can be directly programmed from the relay sequence, programming by anyone familiar with the conventional relay sequence is possible.
(2) Since the princing system is superior to that of a control relay panel, a sequence control system of from 50 to 200 control relays can be economically constructed.
(3) Since each function is modulized and has a plug-in construction, removal and replacement are simple, and maintenance and inspection are easy.
(4) Keyboard type program loader with intelligent functions makes loading and monitoring simple.
(5) Maximum number of inputs and outputs is 64 or 128 channel basic unit and an expansion unit are available. Four different systems having maximum capacities of 64 channels, 128 channels, 192 channels, and 256 channels can be constructed by combining the basic unit and expansion units. Moreover, the number of inputs and outputs can be increased or decreased in 8 channel units according to the control scale.
(6) Both a wall mounted type and a rack mounted type are available for compact control systems.
(7) All external connections are made with screws. Since input and output display and operation are performed at the front, handling is easy.

III. CONSTRUCTION

Various function modules are available to meet a wide range of applications. Consideration has been given so that the ideal configuration for the particular application is possible. The construction of the FUJILOG-μT is shown in *Fig. 2*.

A basic unit or expansion unit having a maximum of

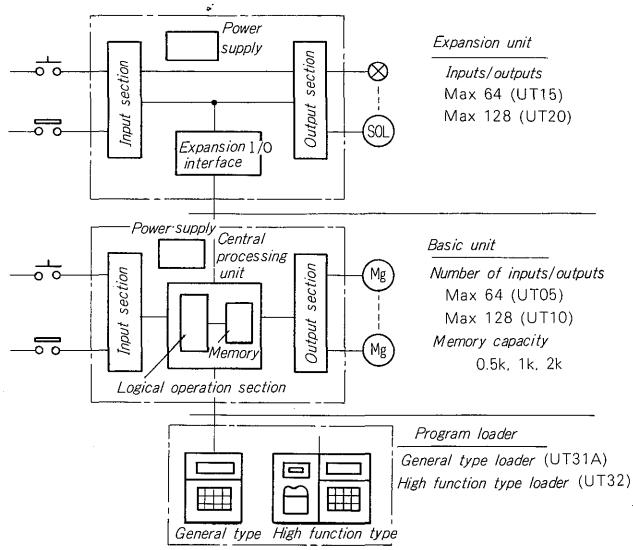


Fig. 2 Construction

64 inputs/outputs and 128 inputs/outputs are available. The basic units consists of a central processing unit (CPU), memory unit (MEM), power supply (PS), and the required number of I/O cards. The expansion unit consists of an expansion I/O interface (EX I/O), power supply (PS), and the required number of I/O cards. Both units are connected by a special cable. Two types of program loaders are available, a general type loader (for RAM) and a high function loader (for RAM & PROM). In addition to the common program writing function, these loaders also have a monitoring function.

Program memory and ARG memory contents, I/O and internal data memory state, and timer and counter current values can be checked while the program is executing (RUNNING). Furthermore, storage of the program contents on cassette tape (CMT), print out of the program list, and writing of the program to PROM is possible with the high function loader.

1. Specifications

The specifications of FUJILOG-μT are given in *Table 1*.

Table 1 Specifications

Item	Specifications	Remarks
Control system	Synchronous control	
Program system	Stored program	Program written by program loader.
Kinds of instructions	4 basic kinds	See Section IV.
Operation system	Cyclic operation	
Processing functions	Logical operation Timer operation Counter operation Shift register operation Step control operation	See Section IV.
Program steps	512, 1,024, 2,048	IC memory
Cycle time	20 ms fixed	
Internal data memory	1,024 points	IC memory
Number of inputs/outputs	Maximum 256	Expanable in 8 channel units, with display.
Kinds of I/O cards	11 kinds	See Table 2.
Self-diagnosis	Internal	
Power requirement	AC 100 V $^{+10\%}_{-15\%}$, 50/60 Hz	
Ambient conditions	0 ~ 45°C (RAM) 0 ~ 55°C (PROM) 10 ~ 85%RH	
Accesory devices	Program loader	Symbolic and decimal keys.

2. Central Processing Unit (CPU Module)

The CPU module consists of an accumulator that performs bit and byte processing, an ARG memory and internal data memory that store the operation results and data, a control circuit that controls these, and a self-diagnosis circuit.

The program memory, internal data memory, I/O cards, and ARG memory are determined by inherent addresses. These are constructed so that signals are exchanged through a data bus in accordance with the contents of the address bus. At program execution, the following four operations are performed by means of commands from the control circuit.

(1) The operation code (READ, AND, etc.) is read from the program memory and stored at the operation code register (OPREG) in the accumulator.
(2) The data of the I/O cards or data memory specified by the operand are stored at the data register (DREG) in the accumulator.
(3) Operation is performed in the accumulator.
(4) The operation results are stored at the I/O card, data memory, and ARG.

3. Program Memory Card

The memory card that store the control program consist of an RAM card that permits easy modification of the program contents and a PROM card having fixed contents. Each instruction consists of 16 bits (of these, 2 bits are parity bits). Memory capacities corresponding to the size of the program are available.

1) RAM card

The RAM card consists of a low power consumption CMOS IC RAM and a floating charge type NiCd battery. Even if the power is turned OFF, the program contents are maintained for more than 2 weeks at an ambient temperature of 45°C by this battery back-up. The battery can be charged from the front of the card without destroying the contents of the stored program.

Parity check and battery voltage check are performed constantly. If the parity or battery voltage is abnormal, the card operation indicator extinguishes and an alarm signal is simultaneously sent to the CPU and operation is immediately halted.

2) PROM card

The PROM card is an erasable PROM by ultraviolet rays that is switched to the previously mentioned RAM when the contents of the program have established. The program is written to the PROM by mounting each card at the high function loader and transferring the contents of the program on cassette tape or an RAM card to these cards. This card can also be used for program storage.

4. I/O Cards

These cards convert the high voltage level input signals to internal logic level at the external control signal interface section through a data bus to the accumulator and convert the operation result to external load drive signals. The card accommodates eight input or output circuits and is connected to the outside through a terminal board at the front. Since LED are provided at the positions corresponding to the terminal screws, the status of the I/O signals can be checked from the front. The cards are color coded by rating at the front to prevent erroneous use.

The internal circuitry is isolated from the outside by a photocoupler and noise immunity has been improved by adding a filter and Schmitt circuit. A wide variety of output switching circuits, such as AC Triac output (AC 100, 200 V) applicable to switching of such frequently switched loads as solenoid valves, relay output, etc., is available.

A C-R type timer card whose operating time is adjustable from the front and a latch relay card having a signal

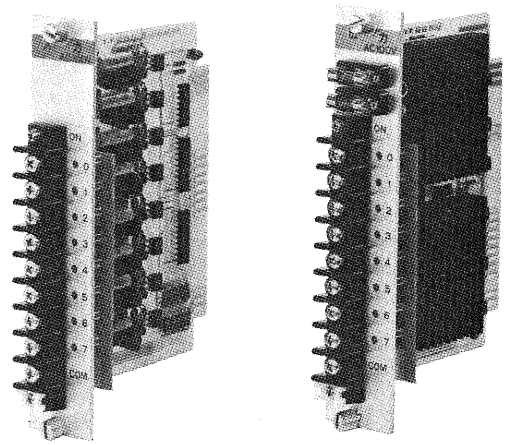


Fig. 3 Exterior view of I/O cards

Table 2 Specifications of I/O cards

Kind	Model	Voltage	Current	Remarks
Input	UT5220	DC24V	typ. 10mA	Operating time approx 20ms
	UT5140	AC100V	typ. 10mA	Resetting time approx 30ms
	UT5150	AC200V	typ. 10mA	
Output	UT5422	DC24V	1mA~2A	Transistor output
	UT5342	AC100V	10mA~2A	Triac output
	UT5352	AC200V	10mA~2A	Triac output
	UT5502		10mA~2A	Fuji E type card relay
Others	UT5702	Dummy	–	Display only
	UT5701	Latch	–	4 channels/card
	UT5703	Switch	–	For test input
	UT5610	Timer	–	C-R type 0.1~10s

hold function at a power failure, input switch card capable of simulating the input, and other special cards are avilable. Exterior views of the I/O cards are shown in *Fig. 3*.

5. Power Supply

Because a simple construction and compact size has been realized through reduced power consumption, unification of the internal voltages, and the use of a switching regulator, the same plug-in construction as the other modules is used. A power switch is provided at the input side of the power supply so that each supply can be turned ON and OFF independently. Moreover, a power supply terminal board which permits powering of the expansion unit and other peripheral devices simultaneously by means of this switch is available.

The entry of noise from the power supply input side is prevented by a line filter and transformer with static electric shield. An overvoltage, overcurrent protection circuit and internal temperature rise detection circuit are provided at the DC side for increased safety. Since an output contact (STX) is ON during normal operation and an output contact is OFF when an abnormality occurs, interlock conditions with other devices can be created.

The functional block diagram of the power supply module is shown in *Fig. 4*.

6. Housing

Two kinds of housings capable of accommodating eight

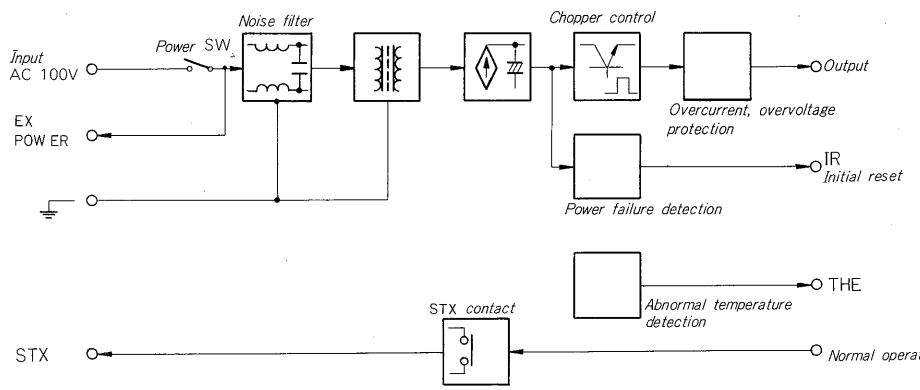
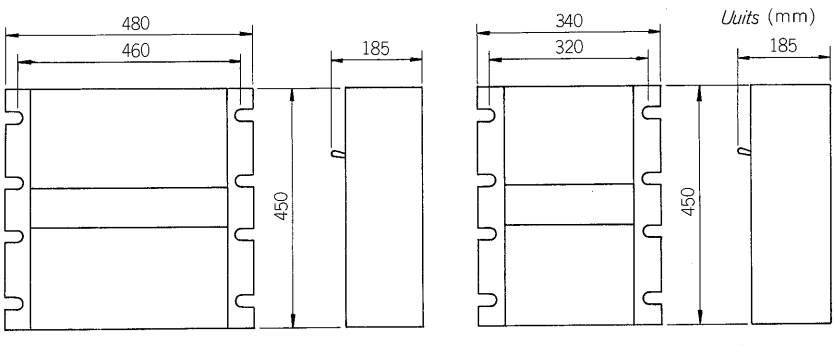


Fig. 4 Block diagram of power supply module



(a) 128 channel housing (b) 64 channel housing

Fig. 5 Outline dimensions

Table 3 Functions of program loader

Function		General type	High function type	Remarks
Programming	Program write	○	○	Operable when the CPU is stopped (PRG). However, program can also be read while the CPU is operating (RUN).
	Program read	○	○	
	Program addition, insertion	○	○	
	Program modification, correction	○	○	
	Program erasure (for RAM)	○	○	
Monitor	ARG memory monitor	○	○	1 bit or 8 bit simultaneously display by decimal point of 8 numerical LED.
	I/O card signal monitor	○	○	
	Data memory monitor	○	○	
	Timer, counter value monitor	○	○	Current value decimal display
Transfer	Copy of program memory by cassette tape (CMT).	–	○	Copying of contents of memory card to cassette tape and transfer from cassette tape to memory card (RAM).
	Print out by printer	–	○	Hard copy of contents of memory card or cassette tape by mnemonic.
	PROM write	–	○	Contents of memory card or cassette tape written to PROM in card units.
Collation		–	○	Collation of contents of memory card (both RAM and PROM) and cassette tape. Results printed at printer.
Operation error detection, display		○	○	Key operation error, undefined instruction check, program step and data address overflow, etc. "Err 0" display.
Operation error detection, display		○	○	Faulty connection to mainframe, program operation while running (RUN), memory write error, CPU malfunction, etc. "Err 1" display.

(64 I/O) or sixteen (128 I/O) I/O cards, CPU, memory and power supply modules are available.

The required number of jacks is arranged at the position at which the cards are mounted. These jacks are interconnected by a bus and wired by a mother board type printed circuit board. If the CPU and memory module are mounted at fixed positions, the housing constitutes the basic unit. The modules and I/O card jack connection system is such that an expansion unit is formed by mounting the expansion I/O interface module in place of these modules.

The outline dimensions of the housing are shown in *Fig. 5*.

7. Program Loader

A general type and a high function type program loader is available. The functions of these program loaders are given in *Table 3*.

In addition to programming and various operations monitoring functions, functions which detect operation error can be incorporated through the use of a microprocessor at the internal circuit.

Normal programming is convenient with the small general type.

Operation is performed in accordance with operation of pushbuttons arranged by purpose. The frequently used basic instruction keys are provided independently as symbolic keys and the function instruction keys are simple keys arranged as single function keys. Operability is improved by handling the various addresses and data specification numbers as decimal numbers.

In addition to the above functions, the high function loader has cassette tape program storage, printer program list creation, and PROM write functions.

IV. PROGRAMMING

1. Programming Preparations

1) Creation of control circuit

Since programming of this programmable controller is performed in accordance with the control circuits based on the design of the control system, first the control circuit diagram must be prepared. The control circuit diagram may be a ladder diagram, logic diagram (logic sequence), etc. However, no matter how it is represented, it is an instruction organization that can be easily programmed.

2) Deciding of addresses

The input and output signals connected to the I/O section of the controller are processed by the program by using unique addresses inherent to the I/O section. Therefore, the connection points of the input and output signals are decided and addresses are assigned to the input and address signals before beginning actual programming. At the same time, the timers, counters, and internal relays, etc. are mapped in the internal data memory and the addresses of all the signals used by the program are decided.

2. Kinds of Instruction and their Operation

1) Instruction format

The instructions of this controller consists of the following three blocks:

[Operation] + [Modification] + [Operand]

Execution instruction control and operation contents are specified at the operation part. The address of the signal to be controlled and operated is specified at the operand part. This may be a bit address corresponding to the instruction (in the case of I/O and logic operation instructions) or a card units byte address (function instruction) and register. The modification part specifies inversion processing of signals. If not signal "N", the signal is processed as N.O. contact.

2) Kinds and operation

Since relay sequence operation is basically contact (bit signal) serial or parallel connection processing, the following four basic operations and control instructions are defined:

R (READ) instruction: This is an input instruction that fetches the first signal of an operation to the controller. The specified bit signal is read to the operation register (ARG) by executing this instruction. The signal already in ARG is transferred to the memory register (MRG) before execution of this read operation.

W (WRITE) instruction: This instruction outputs the result of an operation. The contents of ARG are output to the specified bit address by execution of this instruction. The contents of the ARG remain unchanged after output.

A (AND) instruction: This instruction performs serial connection processing of contacts. The contents of ARG and the bit signal specified by this instruction are AND'ed (serial connection) and the result is stored in ARG by execution of this instruction.

O (OR) instruction: The contents of ARG and the bit signal specified by this instruction are OR'ed (parallel connection) and the result is stored in ARG by execution of this instruction.

Connection processing at the relay sequence can be represented by four instructions described above. However, the following instructions are also defined for time, counting control, step control, etc.

W TMR instruction: This instruction is used when creating a timer by program. The operand of this instruction specifies the card address. Generally, the card address (1 byte, 0 ~ 7 bits) of the internal memory data region is specified. When this instruction is executed, the specified 1 byte memory counts the clock signals (0.1 sec) produced inside the controller, and when the counted value reaches the value specified by the DS instruction, the time up signal is output at bit 7. The maximum settable time is 12.7 seconds. The timer start and enable signals are specified by the program by means of the R instruction before this instruction.

W CTR instruction: This instruction is used when creating a counter by program. The card address of the data region of the internal memory is generally specified at the operand of this instruction, the same as timer. When this instruction is executed, the specified 1 byte memory counts the external clock signals, and when the preset value specified by the DS instruction is reached, a count up signal is output at bit 7.

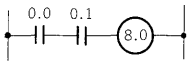
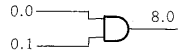
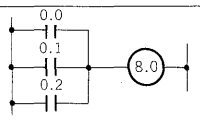
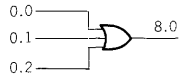
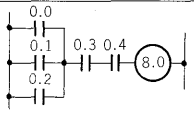
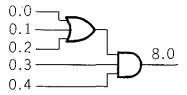
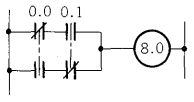
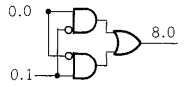
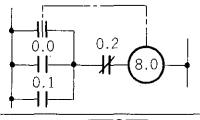
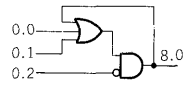
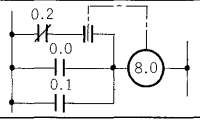
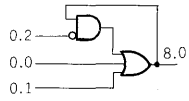
W SR instruction: This instruction is used when creating a shift register by program. The operand generally spe-

Table 4 Instruction list

No.	Basic instruction		Modification	Device*			Remarks
	Function	Symbol		Device modification	Address		
					Card No.	Position	
1	I/O control instruction	R			O	O	Read
2		R	N		O	O	Read Not
3		W			O	O	Write
4	Logic operation instruction	A			O	O	And
5		A	N		O	O	And Not
6		O			O	O	Or
7		O	N		O	O	Or Not
8		A		MRG			
9		A	N	MRG			
10		O		MRG			
11		O	N	MRG			
12	Function instruction	W		TMR	O		Timer start
13		W		CTR	O		Counter start
14		W		SR	O		Shift register
15		W		SC	O	O	Step controller
16		W		NRG			Common interlock
17		W	N	NRG			Common interlock release
18	Others	DS		Set value			Timer, counter set value
19		CLR			O		Card clear
20				Numerical "0" set			NOP

* O indicates number specification.

Table 5 Example of the basic program

Basic circuit	Relay sequence	Logic sequence	Program STEP	Program OPE	Program DEV	Remarks
1) AND *circuit*			0 1 2	R A W	0.0 0.1 8.0	
2) OR *circuit*			0 1 2 3	R O O W	0.0 0.1 0.2 8.0	
3) AND + OR *circuit*			0 1 2 3 4 5	R O O A A W	0.0 0.1 0.2 0.3 0.4 8.0	*Programmed from* OR *circuit.*
4) EXOR *circuit*			0 1 2 3 4 5	RN A R AN O W	0.0 0.1 0.0 0.1 MRG 8.0	
5) *Self-hold circuit (reset priority)*			0 1 2 3 4	R O O AN W	0.0 0.1 8.0 0.2 8.0	0.0, 0.1 } *set input* 0.2 : *reset input*
6) *Self-hold circuit (set priority)*			0 1 2 3 4	RN A O O W	0.2 8.0 0.0 0.1 8.0	0.0, 0.1 } *set input* 0.2 *reset input*

cifies the card address of the data region of internal memory. The specified 1 byte memory is operated as an 8-stage shift register. The shift pulse and shift data are programmed and fetched by R instruction before this instruction.

W SC instruction: This instruction is used when creating a stepping switch function by program. The operand generally specifies the bit address of the data region of the internal memory. The 1 byte memory (bits 0 ~ 7) containing the specified bit operates as an 8 bit exclusive flip-flop and has an 8 step stepping switch function. This instruction may also set and reset the corresponding bit at each step. The stepping conditions are specified separately by program.

W NRG instruction: This is the output batch interlock instruction. When "0" is set in the operation lock register (NRG) by this instruction, the ARG at program execution during this period is fixed at 0 and the outputs become all 0 until the contents of NRG are set to "1" by the next W NRG instruction.

The instructions table of the sequence controller described above is given in *Table 4* and examples of the basic program is given in *Table 5*.

V. CONCLUSION

As introduced above, numerous considerations have been given to the FUJILOG-μT so that it can be easily adopted as a replacement for the conventional relay panel. Favorable comments on its easy programming and handling were received soon after it was placed on sale.