Double Schottky Barrier at Grain Boundary in Ceramic Semiconductors

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1. Introduction

Recent research has indicated that the electric properties of grain boundaries in ceramic semiconductors are related mainly to the double Schottky barrier (DSB) formed at the grain boundary[1] [2]. Therefore, in order to create and design new intelligent ceramic materials it is important to understand the precise role of the grain boundaries. Although Heywang already explained the characteristics of PTC thermistors in 1964 with the DSB model[3], there are still some quantitative discrepancies between theoretical calculations and observed results. The most important reason for the discrepancies is the negligence of the effect of the interface states at the grain boundaries. In this paper a quantitative analysis of the applied voltage dependence of the interface states in a DSB is carried out by simplifying the density distribution of the interface states. This treatment is extended to interpret the electric properties of ZnO varistors and PTC thermistors.

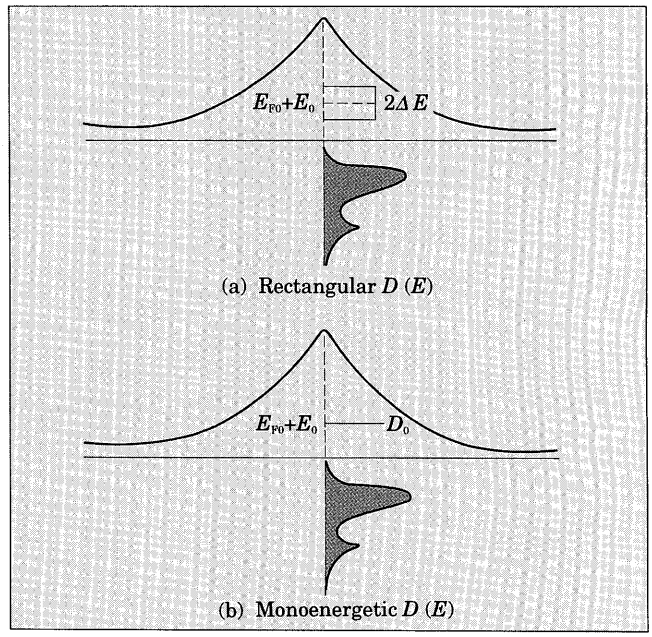
2. Applied Voltage Dependence of DSB

Double Schottky barriers (DSB) are electrical potential barriers formed at grain boundaries of ceramic semiconductors. When a certain voltage is applied, electrons are trapped by the interface states at grain boundaries. The DSB shape is deformed, resulting in a change of barrier height (ϕ). This change has a strong effect on the electrical properties of the ceramic semiconductor. However, it is difficult to determine the quantitative change of ϕ_1 because of the lack of information about the interface states. If we assume the density distribution of the interface states, $D(E)$, to be rectangular as shown in Fig. 1, we can obtain a quantitative ϕ_1-V relation in the following three cases.

(1) $D(E)=0$, $(E>E_{F_0})$
(2) Rectangular $D(E)$[4], $(D(E)=D_0, E=E_0\pm\Delta E)$
(3) Monoenergetic $D(E)$, $(D(E)=D_0$ at $E_0)$

In the case of (1), where there are no interface states above E_{F_0}, the interface charge remains constant and the ϕ_1-V relation can be expressed by the following equation.

Fig.1 Model of distribution function of interface states



$$\phi_1 = (1-\frac{qV}{4\phi_0})^2\phi_0 \qquad \cdots\cdots\cdots(1)$$

In the case of (2), the interface charge is held constant until the Fermi level intersects the bottom of the rectangle similar to case (1). Above the bottom of $D(E)$ electrons begin to be injected into the interface states. The electron injection is completed at the top of the rectangle. Here the interface charge is again kept constant. Numerical analyses of V and ϕ_1 yield the simulated ϕ_1-V relation shown in Fig. 2. This figure shows the results of four simulations.

3. I-V Characteristics of ZnO Varistors

The zinc oxide varistor is one of the most common ceramic semiconductor devices. If the conduction mechanism of ZnO varistors is assumed to be based on the DSB thermoionic process, the current-voltage characteristics are theoretically calculated by the following equation where A is the Richardson constant and T is the absolute temperature.

Fig.2 Calculated ϕ_1–V relation for rectangular $D(E)$

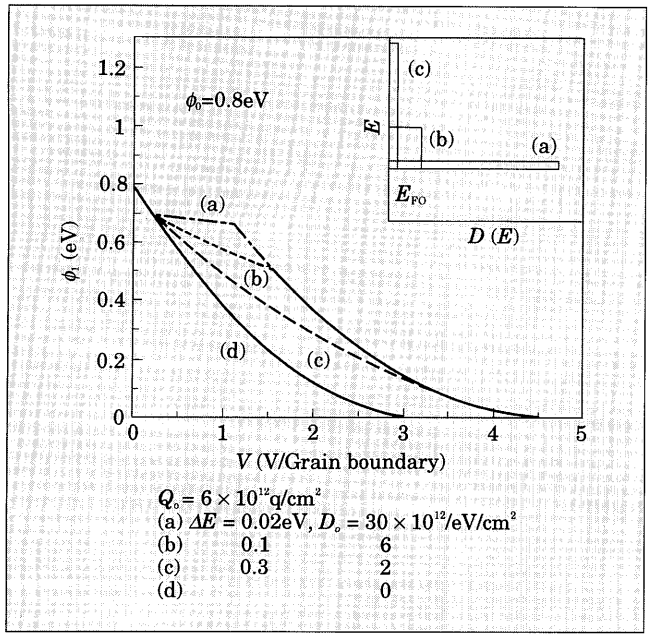
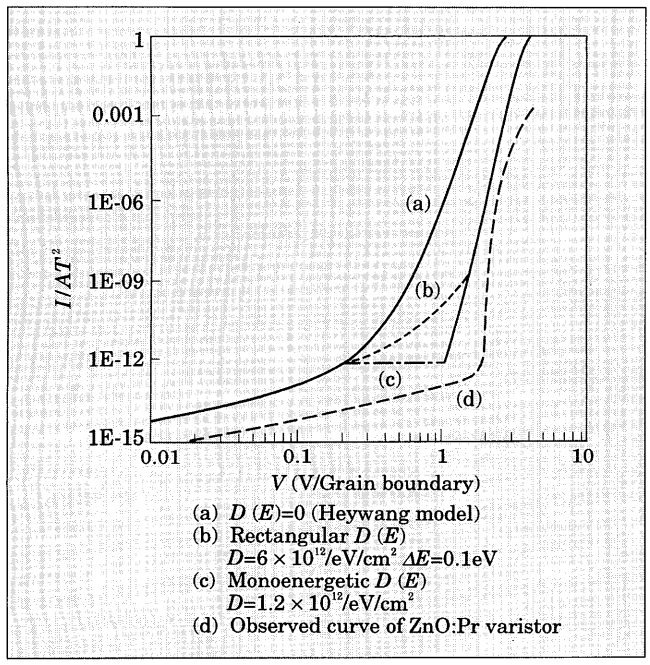


Fig.3 Calculated I–V characteristics of DSB

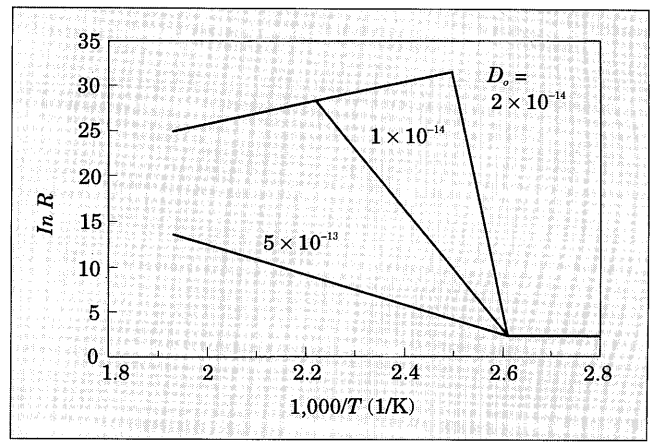


$$I = AT^2 \exp(-\frac{\phi_1}{kT}) \quad \cdots\cdots(2)$$

$$\alpha_{max} = \frac{\phi_0 S_F^{\ 2}}{2kT} \quad \cdots\cdots(3)$$

As shown in Fig. 3, eq. (2) gives I–V curves for the three typical cases discussed above and an observed I–V curve of a ZnO:Pr varistor is also shown. The maximum theoretical nonlinear exponent, α_{max}, is obtained from eq. (3). Although the calculated value of α for a rectangular D (E) was approximately 22, that of the observed curve was more than 80. Therefore the nonlinearity in ZnO varistors should be attributed to the different mechanism from filling of the interface states.

Fig.4 Calculated lnR–1/T relation of PTC thermistor



4. PTC Thermistors

The basic conduction mechanism of PTC thermistors has already been established by early researchers, such as Heywang and Jonker[3),(5)]. However, here we describe the PTC effect with respect to changes in ϕ and the interface charge, Q, where the E_F pinning phenomenon has occurred. When D_o of D (E) is extremely high or D (E) is monoenergetic, E_F is pinned by the interface states. Therefore, the ϕ change near the Curie temperature (θ) can be divided into three regions.

(1) $\ln R = \ln R_o$ (Low resistive region)

(2) $\ln R = \ln R_o + \frac{(qD_o)^2}{8k\varepsilon_o N_d C}(1-\frac{\theta}{T})$ (Curie-Weis region)

(3) $\ln R = \frac{E_o}{kT} + \text{Const.}$ (Pinning region)

Figure 4 illustrates the $\ln R$–$1/T$ relations. From region (2), one can see that the magnitude of the PTC effect depends on D_o, N_d, and θ.

5. Characterization by ICTS Measurement of Electronic Interface States at Grain Boundaries

5.1 ZnO varistors

ICTS (Isothermal Capacitance Transient Spectroscopy) is an intensive method to investigate the interface states in ceramic semiconductors[6),(7)]. This method gives peaks not only for the bulk traps in the grains but also for the interface states at the grain boundaries. Figure 8 shows the observed ICTS peaks generated by applying pulses of various height to a ZnO: Pr varistor. When applied pulses are lower than the varistor voltage, ICTS peaks were observed at the same position. This result indicates that E_F is pinned by the interface states. In addition, the calculated shape of the ICTS peak for monoenergetic interface states coincided with the observed peak. On the other hand when the applied pulses were higher than the varistor voltage, a new ICTS peak appeared at shallower position. This

Fig.5 Observed ICTS spectrum of a ZnO: Pr varistor

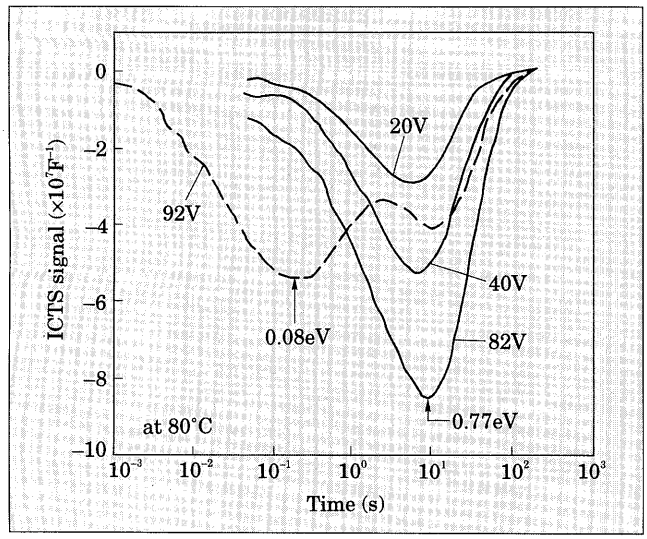
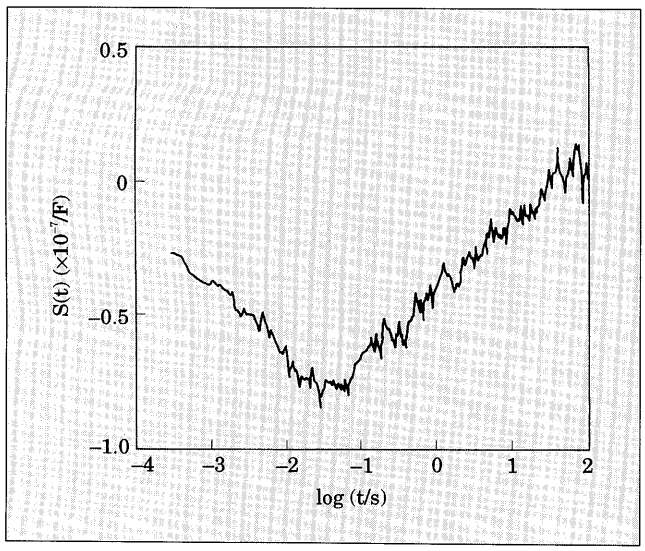


Fig.6 ICTS spectrum for PTC thermistor at Curie-Weis Region
T=175°C

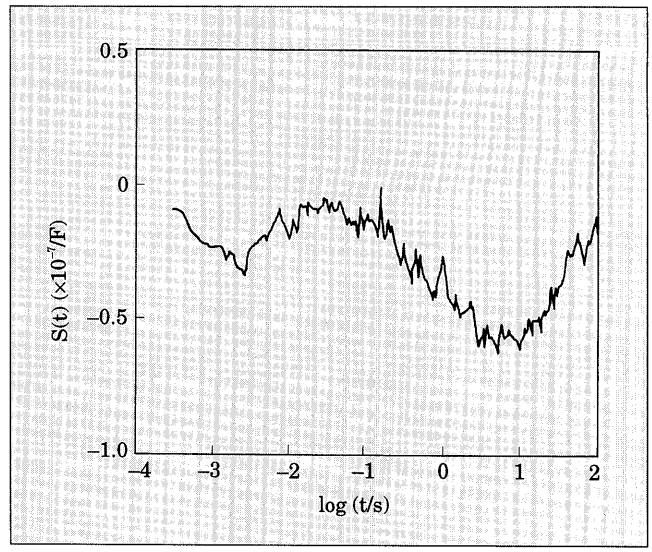


phenomena indicates that E_F is released from pinning through some mechanism which is not yet clear. Therefore highly nonlinear I–V characteristics should be closely related to this release of pinning.

5.2 PTC thermistors

When the ICTS method is applied to PTC thermistors, similar information about interface states can also be obtained. Figure 6 shows the observed ICTS results for a PTC thermistor. Since the temperature of the sample is 175°C, 25°C below the temperature where resistivity becomes maximum, this spectrum indicates the Curie-Weis region. As mentioned before, the Heywang model of PTC thermistors contains no interface states above E_o. Therefore, ICTS measurement should not yield any peaks. However one can find a peak at log t≈–1.5 in Fig. 6. This result shows that some interface states exist above E_o. Figure 7 shows the similar ICTS result at 210°C, where the pinning region

Fig.7 ICTS spectrum for PTC thermistor at pinning region
T=210°C



has already started. Two new peaks appeared at log t≈–2.5 and log t≈1. The quicker peak can be interpreted to have the same origin as that of Fig. 6 because the higher temperature reduced the life time of the interface states. The slower peak in Fig. 7 can be interpreted to correspond with the deep traps at E_o, which pin the Fermi level.

6. Conclusion

The applied voltage dependence of the DSB was quantitatively simulated by simplifying the density distribution of the interface states. It was pointed out that interface states play an important role on the electrical properties of ceramic semiconductors. The calculated results were compared with the observed results of I-V and ICTS measurement to obtain the following conclusions.

(1) The interface states retard the decrease in ϕ_1 and extremely high density interface states will fix the Fermi energy and ϕ_1.
(2) I-V characteristics are influenced not only by energy levels but also by the density and width of the energy distribution.
(3) Although saturation of electron charge into the interface states will produce a steep rise in current, its nonlinear exponent, α, is confined to 22. Another mechanism is needed to explain the high nonlinearity in ZnO varistors.
(4) The PTC effect can be quantitatively understood by taking interface states into account based on the DSB model.
(5) ICTS measurement of the ZnO:Pr varistor showed that the Fermi level of the ZnO grains is fixed by the interface states and that the interface states are distributed monoenergetically. These results agreed with the calculated results of the DSB structure. Moreover, an applied voltage higher

than the varistor voltage released pinning of the E_F and brought about a different conduction mechanism which should be the cause of highly nonlinear I–V characteristics.

(6) ICTS results of the PTC thermistor showed the existence of interface states above the deep traps at E_o. The peak corresponding to deep traps appeared at log $t \approx 1$ at higher temperature.

7. References

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