# A New Semiconductor Device with Trench Technology

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## 1. Introduction

Fuji Electric has advanced the development of semiconductor processes by promoting the research and development of "genuinely controlled processes that do not generate defects" and "devices having decisive advantages over the competition." Using specialized equipment and concentrating on processes that involve chemical reactions such as oxide layer, etching and thin film deposition and are susceptible to problems, and by making full use of microscopic analysis techniques and pursuing the true causes of problems, Fuji Electric has realized semiconductor processes having high reliability and low defect rates.

By maximizing the usage of silicon (Si) in three-dimensions in order to bypass characteristics limits of planar on-resistance, breakdown voltage and the like, and by positioning trench technology as a core technology, Fuji has promoted the research and development of the usual trench MOSFET and also new semiconductor devices such as the trench lateral power MOS (TLPM), super junction (SJ) device, and a 700 V-class trench offset drain-lateral DMOS (TOD-LDMOS).

TOD-LDMOS is a new semiconductor device and is the first application of trench processing and the concept of using a silicon substrate in three-dimensions in order to realize high breakdown voltage. This paper describes the key supporting process technologies of trench etching technology, CVD (embedding, flattening) technology and gate oxide layer (deposition, high breakdown voltage) technology that have been developed by Fuji Electric.

## 2. Structure of the New Semiconductor Device (TOD-LDMOS)

In the past, a structure (offset drain area) capable of realizing a breakdown voltage of 700 V or higher required an area of approximately 60 μm length on the substrate surface as shown in Fig. 1. This is because elongation of the depletion layer ($X$ μm) in an n-type area of low concentration can achieve a high breakdown voltage $V = \int E\,(X)\,dx$ (where $E$ is constant, and $V$ is large when $X$ is large) without the maximum electric field ($E_{max}$ V/μm) generated in the vicinity of the junction exceeding the electric field ($E_c$ V/μm) at which a reverse current begins to flow through the Si substrate. $V$ has the theoretical limit of $V < E_c \cdot X$, and $X$ cannot be made shorter because this distance is absolutely essential in principle for achieving the breakdown voltage.

As shown in Fig. 2, with this new technology, a trench of depth 20 μm and width of 20 μm is formed in the silicon substrate and a U-shaped offset drain is provided along the trench to fully utilize the substrate in three-dimensions, ensure the necessary distance, and increase the level of device integration while maintaining a high breakdown voltage.

Figure 3 shows the potential distribution of the TOD-LDMOS device (spacing of the equipotential lines indicates the strength of the electric field). With an offset drain that runs alongside the trench, this structure realizes an electric field within the Si substrate that is rather uniformly relaxed, and because the maximum electric field exists in the oxide

Fig.1 Schematic cross-section of a conventional 700 V-class high voltage lateral MOS

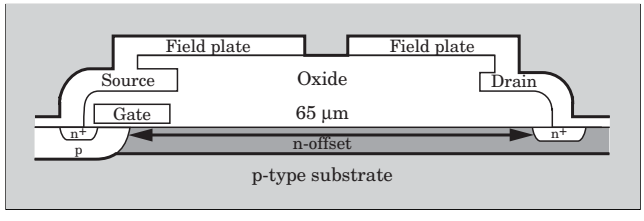



Fig.2 Schematic cross-section of the 700 V-class high voltage lateral MOS with trench technology

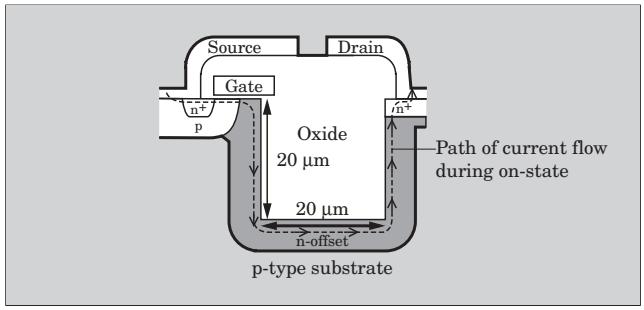
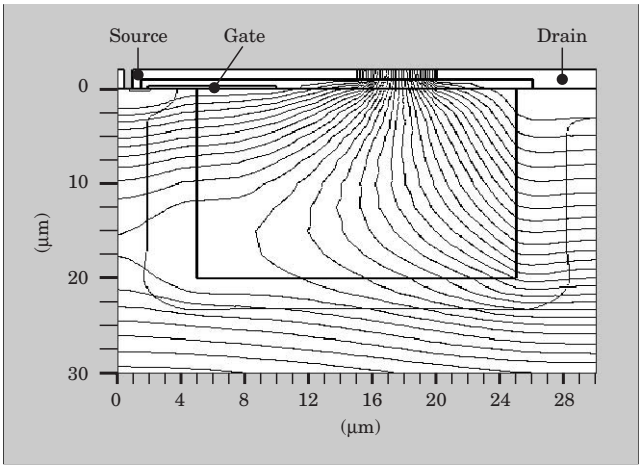


Fig.3 Simulated potential contours of TOD-LDMOS (bias voltage = 600 V, 20 V per contour)




layer which has a higher breakdown voltage than Si by a magnitude of 10, breakdown does not occur even if the linear distance is short.

With this structure, however, it is necessary to form a trench that is deep and wide (20 μm × 20 μm) in the Si substrate, and then within that trench, to form a high-quality insulating region that does not cause a decrease in breakdown voltage. It is also necessary to form an offset drain region by diffusing the trench wall with a low concentration of ions. Such processing is difficult to realize, however. The desired device structure was realized by using a proprietary manufacturing method in which stripe-shaped trenches having a high aspect ratio are fabricated, oblique ion implantation is performed, and then oxidation and CVD processing are implemented to fabricate an insulating film.

## 3. Key Process Technologies for TOD-LDMOS

The key technologies of trench processing are described below.

(1) Formation of stripe-shaped trenches having a high aspect ratio

Figure 4 shows the shape of the trenches. Instead of forming a 20 μm × 20 μm oxide region all at once, several stripe-shaped trenches of width 1.4 μm and depth 20 μm are formed in the source-drain direction to form a sub-divided region at the realizable film thickness. We developed the following essential trench etching techniques to obtain this shape.

- ○ Side wall angle ≈ 90°
- ○ Absence of Si column residue
- ○ Trench side wall protection

Trench etching, as shown in Fig. 5, is performed while protecting the side wall with the derivative product ($SiO_2$) formed in the reaction between oxygen ($O_2$) contained in the etching gas and the Si substrate. At a depth of 20 μm, however, the derivative product generated at the bottom surface will be unable to

Fig.4 The silicon trench etching pattern (depth = 20 μm)

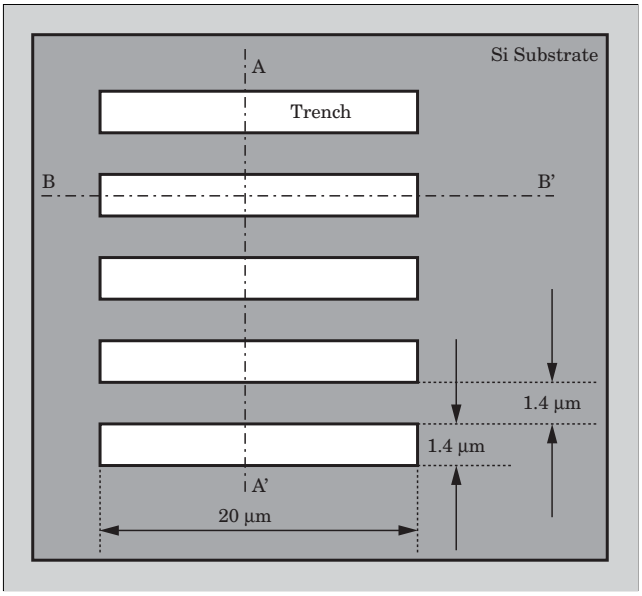
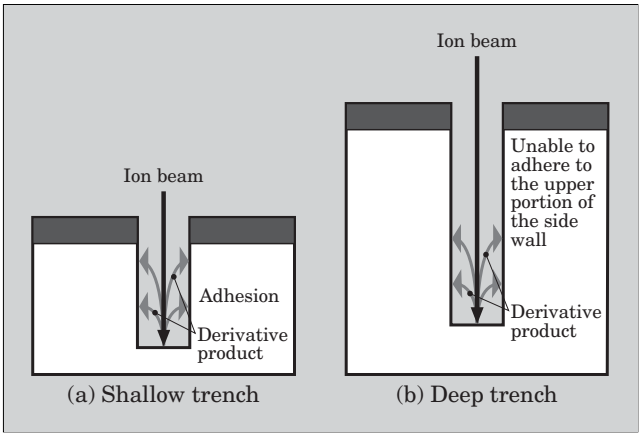



Fig.5 A schematic cross-section of a trench etching




adhere to the upper portion of the trench, and etching will be performed not only on the bottom surface, but also on the upper side walls. Moreover, as the etching depth increases, derivative product generated at bottom surface is not removed, and Si column residue is likely to exist. Therefore, in order to protect the sidewalls, the bias voltage applied to the Si substrate is boosted to increase the rectilinear propagation of the ion beam and reduce the portion of the beam incident on the sidewalls. Additionally, to suppress the generation of derivative products, the fluorine content of the gas is optimized to decompose solid $SiO_2$ into gaseous $SiF_4$ and $O_2$ to make exhausting easier. As a result, a suitable shape for this device can be obtained.

(2) Offset drain fabrication using oblique ion implantation

As shown in Fig. 6, oblique ion implantation and then thermal diffusion are performed along the trench to create an offset drain region in the trench sidewall.

Using the fact that the trench opening is long in the sideways direction, impurities are introduced by

Fig.6 Schematic cross-section of the oblique and vertical ion implantation, followed by offset drain thermal diffusion

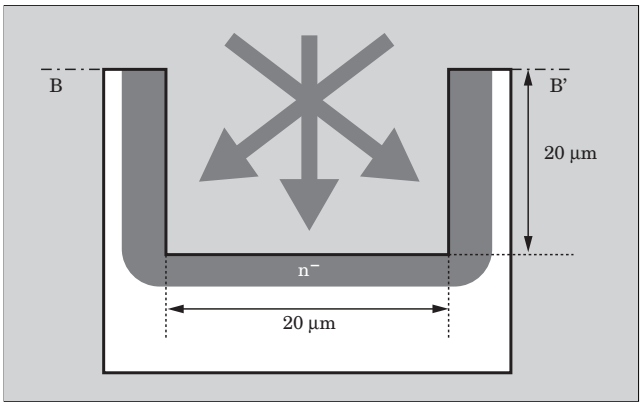



Fig.7 Oxidation of thin crenellated silicon

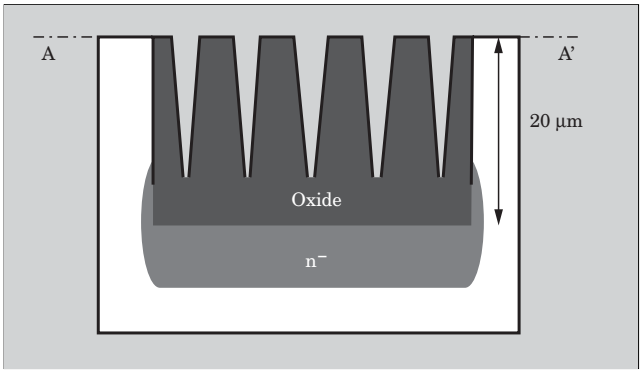
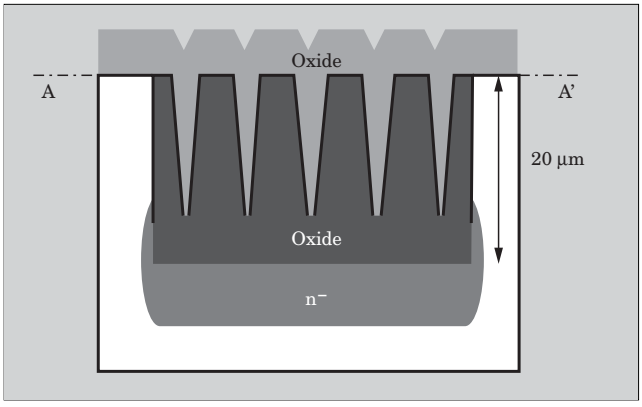



Fig.8 Deposition of oxide in the trench region




implanting ions in a direction horizontal to line segment BB' such that ions will be implanted in the bottom surface and both sidewalls at a 45° oblique angle with relatively low fluctuation.

(3) Thermal oxidation of Si substrate material remaining between crenellated trenches

Figure 7 shows a cross-section of the thin crenellated Si substrate after thermal oxidation.

All Si material between the crenellated trenches has become oxide film ($SiO_2$), and the volume of $SiO_2$ is approximately twice that of Si. At this point in time, gaps will exist at the top of the crenellated substrate. Techniques for scientifically and accurately controlling

Fig.9 SEM micrograph of the fabricated TOD-LDMOS

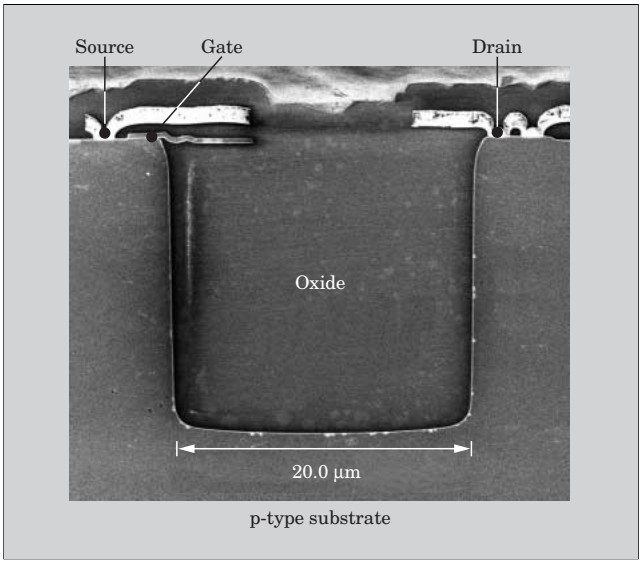
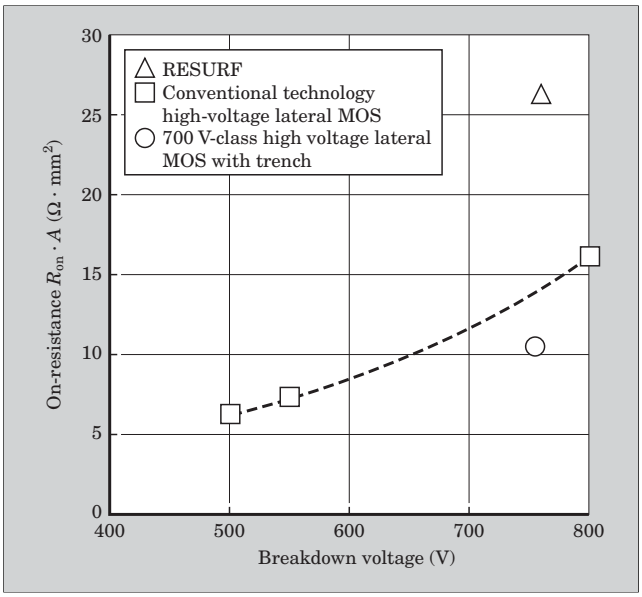



Fig.10 Relationship between specific on-resistance and breakdown voltage




the width of the residue of this thermally oxidized pitch and for relieving stress enable the crenellated shape to be formed without remnants of the Si core and without deformation and collapsing of the oxide film columns by the stress.

(4) Deposition of insulating film in the trench region

Figure 8 shows a cross-section of the Si substrate after deposition of an insulating film.

When insulating film ($SiO_2$) is deposited so as to fill up the gaps, it is important to control empty regions occurring within the deposited $SiO_2$ as stress-relief regions and to deposit the insulating film below the Si surface (line segment AA'). Figure 9 shows a cross-sectional photograph of an actually fabricated TOD-LDMOS device.

As a result, the output on-resistance is reduced by

approximately 30 % compared to prior devices to realize 11 Ω·mm², which is the best in the industry for a device having a 750 V breakdown voltage (Fig. 10). Shrinking the device pitch enables the chip size to be reduced and the production cost of single-chip power ICs to be decreased. It is believed that these techniques will enable cost reductions in such electronic equipment as AC adapters.

## 4. Conclusion

In order to continue developing new devices that utilize Si in three-dimensions to the maximum extent possible, we intend fully to utilize epitaxial growth, embedding and interconnect technologies, as well as trench technology. Moreover, utilizing quantitative process design aided by the analysis of elementary process steps, visualization techniques and in-line evaluation of the etching process, enhanced washing and surface treatment technology, particle component analysis, clean room monitoring technology, and the like, we intend to revolutionize manufacturing processes, enhance the process technology of the Fuji Electric Group and contribute to the development of new products.

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