Trench SBD-Integrated SiC-MOSFET To Suppress Bipolar Degradation

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ABSTRACT

When the body diode of a SiC-MOSFET is forward biased, characteristic degradation occurs as on-voltage increases with stacking faults expanding within the drift layer. To avoid the issue, integrating a trench SBD into a conventional SiC trench gate MOSFET will suppress a body diode current under forward bias without the need for increased chip size. This structure has increased the current density at which characteristic degradation occurs by approximately four times compared with conventional SiC trench gate MOSFETs. Without using external SBDs, this technology is expected to reduce the size and weight of products and reduce characteristic degradation, improving long-term reliability.

1. Introduction

In recent years, there has been growing demand for low-loss power conversion equipment to help achieve a decarbonized society. Compared with silicon (Si), silicon carbide (SiC) has a wider band gap and a higher breakdown electric field. Therefore, it has enabled to reduce resistance of the drift layer due to a thin and high carrier concentration. In addition, its high thermal conductivity and wide band gap allow the device to operate at high temperatures, thus streamlining the cooling system and benefiting power conversion equipment through size and weight saving. For example, in electric vehicles, the use of SiC power semiconductor devices enables inverters to be smaller and lighter and also extends the driving range by reducing losses. Power conversion equipment such as inverters use metal-oxide-semiconductor field-effect transistors (MOSFETs) and Schottky barrier diodes (SBDs). There is a known way to reduce the size of inverter circuits is to reduce the number of devices by using parasitic pn diode (body diode) in the MOSFET instead of external SBD as a free wheeling diode. However, the current flowing through the body diode of the SiC-MOSFET can increase losses due to the on-state voltage increase (bipolar degradation).

This paper will describe the suppression of bipolar degradation in SiC-MOSFETs through the integration with a trench SBD.

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2. Bipolar Degradation and Integrated SBD Suppression Effect

Figure 1 shows the cross sectional viewing of a SiC trench gate MOSFET device. It has been reported that when the current flows through the body diode formed around the trench gate, the forward voltage V_F and the voltage V_{on} at the start of operation, which are applied between the drain and source of the MOSFET, increase due to bipolar degradation.(1) Bipolar degradation is caused by a stacking fault (SF) expanding and forming a high-resistance layer under forward current stress. When the body diode is activated, electrons are injected from the drain side and holes are injected from the source side into the drift layer and substrate. The energy released by the recombination of injected electrons and holes causes the SFs to expand starting from the basal plane dislocation (BPD) present in the drift layer and substrate.(2)

The BPD is a dislocation defect that exists in SiC substrate. It is converted to a threading edge dislocation (TED) at the interface between the drift layer and

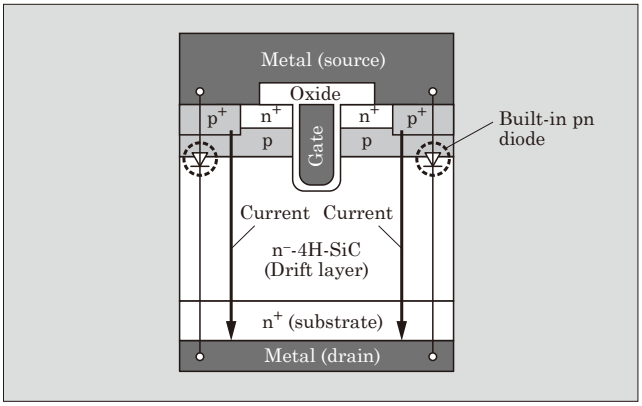

Fig.1 Cross section of a SiC trench gate MOSFET device

the substrate at the start of the epitaxial growth of the drift layer. A SF extends from the BPDs that penetrate the drift layer without being converted to a TED. SFs reportedly extend also from BPDs that has been converted to TEDs under a high current.(3)

Figure 2 shows the graph of ΔV_F versus forward current density up to 500 A/cm² in a conventional SiC trench gate MOSFET, where ΔV_F is a variation from the initial V_F, a voltage before the current stress. With no measures in place, ΔV_F increased when forward current was applied at a current density of 500 A/cm², showing bipolar degradation occurred.

Fuji Electric has developed a recombination promoting layer as a technology to suppress bipolar degradation. In the recombination promoting layer, which is a high carrier concentration layer formed between the drift layer and the substrate, minority carrier holes exhibit short carrier lifetime. Therefore, the number of holes injected from the drift layer into the substrate decreases, suppressing the expansion of SFs. In the future, power devices are expected to become smaller in chip size. To use them at higher current densities, their recombination promoting layer will need to be optimized for highly concentrated and thick film. In addition, we considered it effective not to activate the body diode and not to recombine electrons and holes as an alternative means of suppressing bipolar degradation. As a method to suppress bipolar degradation, this paper studies to integrate SBDs and MOSFETs into one chip (trench SBDs are incorporated).

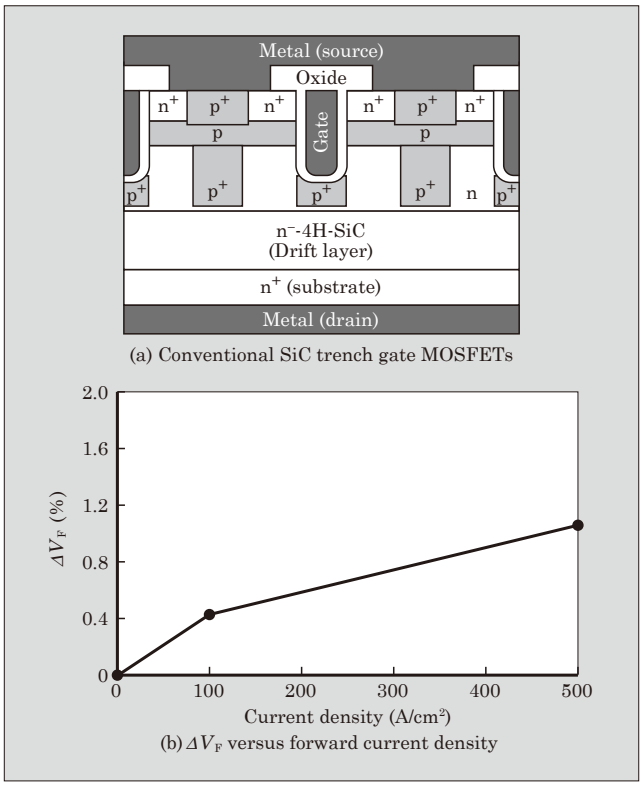

Fig.2 Conventional SiC trench gate MOSFET and bipolar degradation

Next, we will describe the principle of bipolar degradation suppression using an integrated trench SBD. Figure 3 shows the cross-sectional structure of the SiC trench gate MOSFET and the equivalent circuit when activating the body diode. The p-type layer under the SiC trench gate MOSFET and the trench SBD are each connected to the source through the surface p-type contacts in the depth direction (not shown in the figure). The equivalent circuit in Fig. 3 shows the current pathway when the body diode is activated. In contrast to the SiC trench gate MOSFET in Fig. 3(a), the SiC trench gate MOSFET with an integrated trench SBD (SBD-integrated MOSFET) in Fig. 3(b) has a trench SBD and built-in pn diode connected in parallel to share the resistance of drift layer. Although the parallel connection results in equal voltages applied to the trench SBD and the built-in pn diode, the trench SBD is actually formed at a far from the branch point in Fig. 3(b) than the built-in pn diode. We must thus take into account of the resistance between the SBD and the drift layer (spreading resistance). The voltage V_{pn} applied to the built-in pn diode shown in Fig. 3(b) is equal to the sum of the voltage V_{SBH} applied to the SBD and the voltage V_{sp} applied to the spreading resistance. Therefore, if the sum of V_{SBH} and V_{sp} is lower than the built-in voltage V_D of the built-in pn diode, the built-in pn diode will not turn on. V_{SBH} is generally deter-

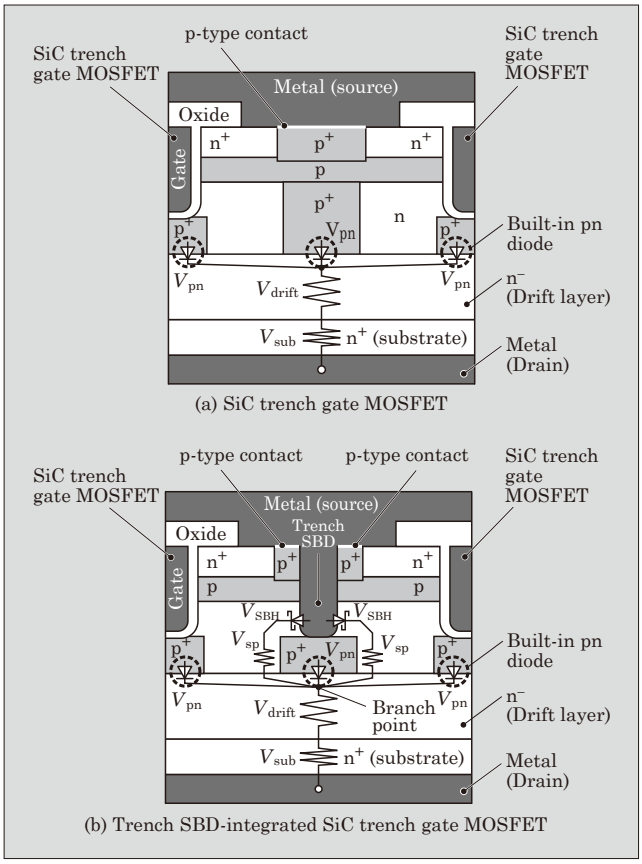

Fig.3 The cross-sectional structure of the SiC trench gate MOSFET and the equivalent circuit when the body diode is activated

mined by the potential barrier height at the Schottky junction and is smaller than V_D. Therefore, adjusting the V_{sp} suppresses the activation of the built-in pn diode. Instead of the built-in pn diode, the trench SBD, a unipolar device, is activated but does not cause bipolar degradation.

3. Characteristics of SiC-MOSFETs with Integrated Trench SBDs

We have established a technology and developed a prototype to form a trench SBD in a SiC trench gate MOSFET by participating in a research project of the joint research body Tsukuba Power-Electronics Constellations (TPEC). For the integration of a trench SBD, forming a planar SBD in conventional SiC trench gate MOSFETs, which have narrow cell pitch, causes wider cell pitch and increases V_{on}, resulting in higher loss. To avoid widening the cell pitch, we formed trench SBDs.

Figure 4 shows a cross-sectional scanning electron microscopy (SEM) image of a prototyped 1,200-V SiC trench gate MOSFET with an integrated trench SBD. We confirmed that a trench SBD was formed between the trench gates of the SiC trench gate MOSFET.

Figure 5 shows the breakdown voltage and current waveforms of a conventional SiC trench gate MOSFET and an SBD-integrated MOSFET at room temperature. It shows that both structures had break down voltage of over 1,200 V. There was no significant difference in the leakage current between the drain and the source, and we confirmed that the leakage current was not affected by the SBD-integrated MOSFET. Figure 6 shows the trade-off between specific on-resistance $R_{on} \cdot A$ and threshold voltage V_{th} at room temperature for a SiC trench gate MOSFET and SBD-integrated MOSFET with the same cell pitch. The gate structure, cell pitch, and active region size remain the same for both structures, resulting in almost identical characteristics.

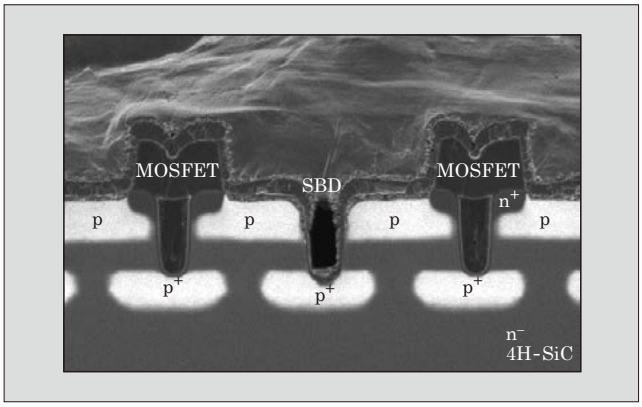

Fig.4 Cross-sectional SEM image of Trench SBD-integrated SiC trench gate MOSFET

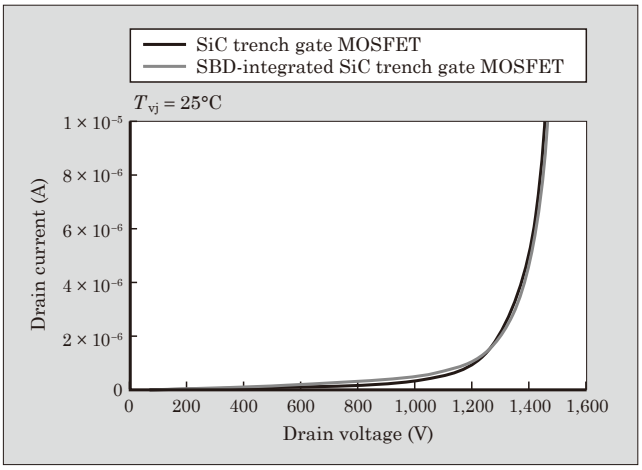

Fig.5 Breakdown voltage and current waveforms

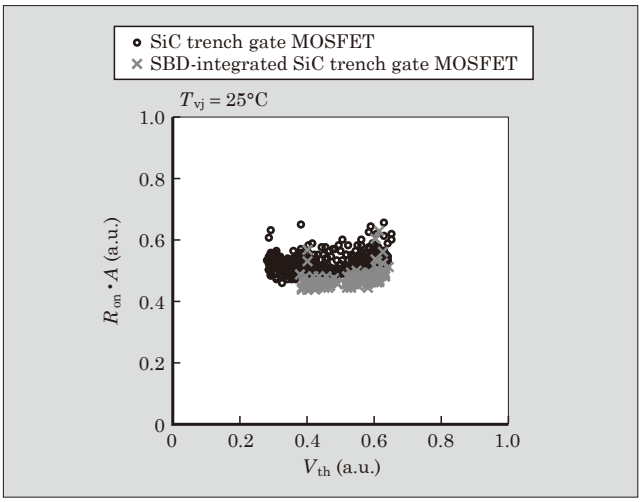

Fig.6 $R_{on} \cdot A$-V_{th} trade-off

4. Verification of the Bipolar Degradation Suppression Effect

Figure 7 shows the J-V characteristics of the body diode at 150°C for a conventional SiC trench gate MOSFET and three types of SBD-integrated MOSFETs with different cell pitches. The cell pitch becomes narrower in the order of device A, device B, and device C.

First, for the conventional SiC trench gate MOSFET, when the built-in pn diode operates, bipolar currents, which consists of electron current and hole current, flows, resulting in exponentially increasing as shown in Fig. 7(a). In contrast, Figs. 7(b), 7(c), and 7(d) show linear characteristics at the initial increase of the J-V waveform. We suppose that V_{SBH} is smaller than the built-in voltage of the built-in pn diode, which activates only the SBD alone, resulting in only unipolar current, namely electron current. For devices A, B, and C, the current density tended to increase steeply as the applied voltage increased. It is thought that the built-in pn diode began to operate, following the trench

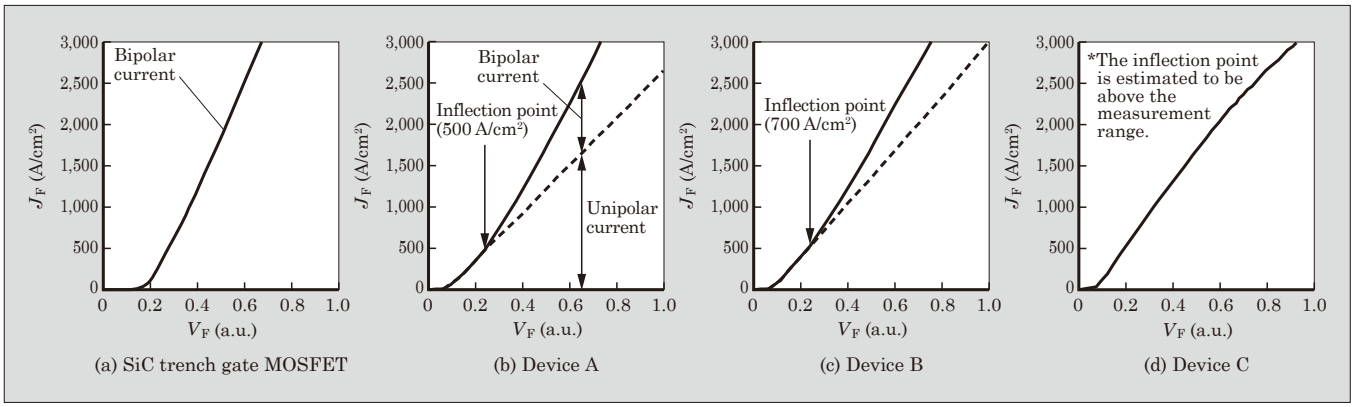

Fig.7 *J-V* characteristics of body diode at 150°C

SBD, at the boundary of the condition (inflection point) where the slope of the current increase changes rapidly. The current density at the inflection point tends to increase as the cell pitch becomes narrower. As the cell pitch narrows, the distance between the branch point in Fig. 3(b) and the SBD becomes shorter, the spreading resistance decreases, and V_{sp} decreases. As a result, it is assumed that the built-in pn diode became difficult to turn on. From the characteristics in Fig. 7(d), it is estimated that bipolar degradation does not occur in device C, which has the narrowest cell pitch, at a current density of 3,000 A/cm² or higher, which is six times higher than that at which bipolar degradation occurs in a conventional SiC trench gate MOSFET.

Next, we conducted a forward current stress test on the SBD-integrated MOSFETs to verify the suppression effect of bipolar degradation. We tested device B and device C to verify the effect before and after the inflection point and to verify whether bipolar degradation occurred at a current density of up to 2,000 A/cm², which is the highest value of the testing equipment. First, we heated device B to 150°C, which is the assumed operating temperature, and applied pulse current with an adjusted duty ratio to suppress the heat generation. After measuring the initial characteristics, we applied current to the devices at 300 A/cm², 700 A/cm², 1,000 A/cm², 1,500 A/m², and 2,000 A/cm². The effective conduction time was 5 minutes for up to 1,000 A/cm² and 2 minutes for 2,000 A/cm². We measured V_F again after forward current stress test and evaluated ΔV_F.

Figure 8 shows ΔV_F versus applied forward current density. We confirmed that there was no increase in ΔV_F under current density lower than 700 A/cm² at the inflection point. At current densities above 1,000 A/cm², we confirmed that ΔV_F increased and the characteristics degraded. Since the bipolar current component increases as the current density increases under conditions above the inflection point, the number of electrons and holes injected into the drift layer increases, leading to bipolar degradation. To check the degraded device for the presence of SFs, we peeled

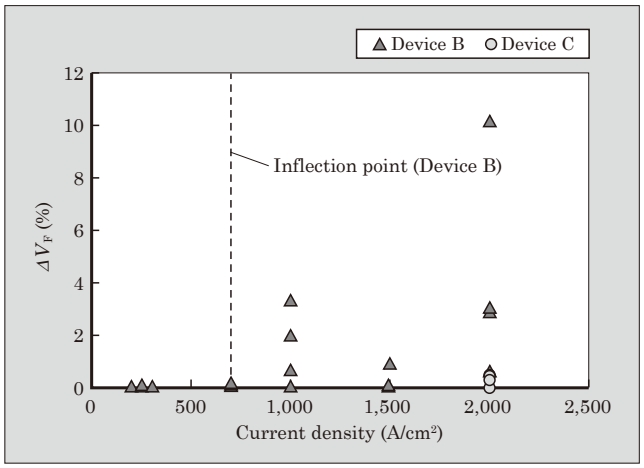

Fig.8 ΔV_F versus forward current density

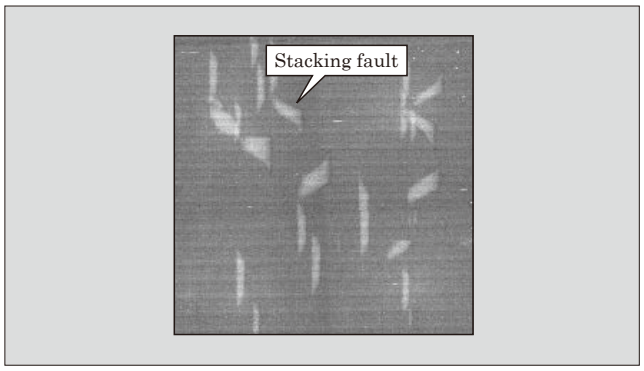

Fig.9 PL image of device with increased ΔV_F after forward current stress

off its surface electrode to perform photo luminescence (PL) imaging measurement at a wavelength of 420 nm, where SFs emit light. Figure 9 shows the PL image of the device with increased ΔV_F after forward current stress. The area shown in white in Fig. 9 corresponds to the expanded SFs. Based on these results, we confirmed that bipolar degradation does not occur near the inflection point where the bipolar current component is small and at current densities lower than the inflection point because either the amount of electron and hole injection into the drift layer is small or the built-in pn

diode does not operate.

After this, we conducted a forward bias stress test on device C, which exhibited an inflection point of higher current density. From the J-V waveform in Fig. 7(d), it can be inferred that ΔV_F does not fluctuate even at a current density of 2,000 A/cm^2. We then conducted a test on device C with an effective conduction time of 2 minutes at 175°C and 2,000 A/cm^2, the most severe conditions of the testing equipment. As shown in Fig. 8, device C showed no bipolar degradation under the most severe conditions in the test environment. The results demonstrated that by increasing the current density at the inflection point by reducing the cell pitch, the characteristics do not degrade at a current density of up to 2,000 A/cm^2, four times that at which conventional SiC trench gate MOSFETs have bipolar degradation.

5. Threading BPD Density Impact Evaluation

Next, we evaluated the dependence of SF expansion on the threading BPD density. We prepared substrates with different BPD densities from several vendors and formed epitaxial film on them to make experimental SBD-integrated MOSFETs. We used them to verify whether the same effect of bipolar degradation suppression could be achieved. We especially tested the selected chips that include threading BPDs by performing PL imaging measurements to evaluate surface distribution of threading BPD in the drift layer that is formed on the epitaxial substrate for the prototypes. The device structure was the same as that of device C, which did not experience bipolar degradation in Section 4. After the initial measurement, we applied a forward DC of 100 A/cm^2 for 10 minutes at 150°C and a pulse current of 2,000 A/cm^2 for 2 minutes at 175°C to the prototypes.

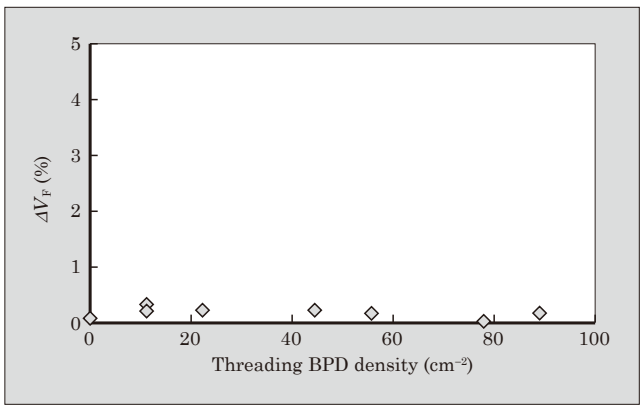

Fig.10 ΔV_F versus threading BPD density

Figure 10 shows ΔV_F versus threading BPD density contained in each chip. For all the evaluated devices, we confirmed that the amount of fluctuation was small compared with initial value before activation and that there was no degradation of the characteristics. The results demonstrate that integrating an SBD is effective in suppressing bipolar degradation, regardless of the density of the threading BPD.

6. Postscript

We conducted research on a structure that integrates an SBD in a MOSFET as a technology to suppress bipolar degradation caused by body diode activation. By using a trench SBD structure, the SBD can be integrated with the characteristics no less than that of the conventional SiC trench gate MOSFETs.

We estimated the current density at which bipolar degradation is suppressed from the inflection point indicated by the J-V characteristics of the body diode. Based on the evaluation, we showed that the narrower the cell pitch, the higher the suppression effect. Actual forward bias stress tests have demonstrated that no characteristic degradation occurs up to a current density of 2,000 A/cm^2, which is four times the current density at which bipolar degradation occurs in conventional SiC trench gate MOSFETs. We also confirmed that bipolar degradation can be stably suppressed regardless of the threading BPD density of the epitaxial substrate.

This research was conducted as a project of the joint research body Tsukuba Power-Electronics Constellations (TPEC). We would like to express our gratitude to Shinsuke Harada and Tadao Morimoto of the National Institute of Advanced Industrial Science and Technology (AIST) for their cooperation in prototyping, evaluation, and consultation.

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