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MICREX-F 100 SERIES

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1 FOREWORD

MICREX-F100 Series (hereinafter abbreviated as F100 series) is situated as medium-order processor among MICREX -F Series (hereinafer abbreviated as F series) programmable controller having a compact structure, and is developed with an aim of applying to the high-function sequence control field for which medium scale and high-speed processing are required.

As F100 series, three types of processors, namely, FPK100, FPK105 and FPU100 are available. All of them, as the standard practice, have 512 input/output points. Though there is no difference in fundamental arithmetic computation capability for control, FPK105 are provided with inter-processor link function, while FPU100 are provided with a bay in which processor and PIO module are mounted as a single unit.

In this series, many new architectures such as, to cite one example, effective connection and execution with exclusive LSI of rudder diagram language which is an improved version of EPOL (program language for Fuji Electric's PC's of MICREX-E Series), have been adopted and on basis of our experience with both series of FUJILOG and MICREX-E Series, various know-hows have been introduced to the system to make it easier to operate.

2 FEATURES OF F100 SERIES

FPK100/105 and FPU100 have, in addition to the unified architecture of F Series, the following features:

2.1 High-speed processing

By adopting LSI's of exclusive use for computationg processing unit, processor function, in particular, that of bit operation is made as speedy as 1 μs/contact. So that, the system can be applied for sequence control of machines for which high-speed response is required with ample margin.

2.2 Possibility of architecturing step-by step controls up to medium scale

The standard proctice is for a total of 512 input/output points (expansible up to the maximum of 1,600 points), but the series is expansible by each 16 points or 128 points.

2.3 Wide-ranged command language

In this series, a new language was adopted so that it can be adopted for new automatization system such as FA and FMS (Flexible Manufacturing System) by enhancing more step sequence command, numerical operation command and filing command, compared with the conventional FUJILOG series that have been widely used for small and medium scaled control system. As arithmetical operations of BCD 8 digits are aimed at by standard type, in proctical use, there is no need to worry about taking a figure up or overflowing, so that handling of numerical values in application program is made easier.

3 SYSTEM CONFIGURATION AND SPECIFICATION

3.1 System configuration

An example of system configuration of F100 series is shown in *Fig. 1*. Three types of processors of F100 series, are provided with, respectively, a 1-circuit terminal link (T link) interface function, through which it can be connected to various PIO capsules, function capsules and program loaders. Further more, FPK105 is providing with a coupling function with processor network (P link), through which data linking with other controllers is possible. FPU100 is a combined unit of processor module and PIO, and with this reduction of mounting space and cost can be expected when input/output signals are cencentrated in one place.

3.2 Specifications

Specifications of F100 series are as shown in *Table 1* below.

4 CONTROL SYSTEM AND OPERATION

4.1 Control system

The global operation of FPK100/105 and FPU100 is controlled by firm ware of high-function micro-processor (hereinafter called CPU). Execution of application program is made in high speed by bit processor of exclusive use for executing directly the indication of rudder diagram, and

Fig. 1 System configuration of F100 series

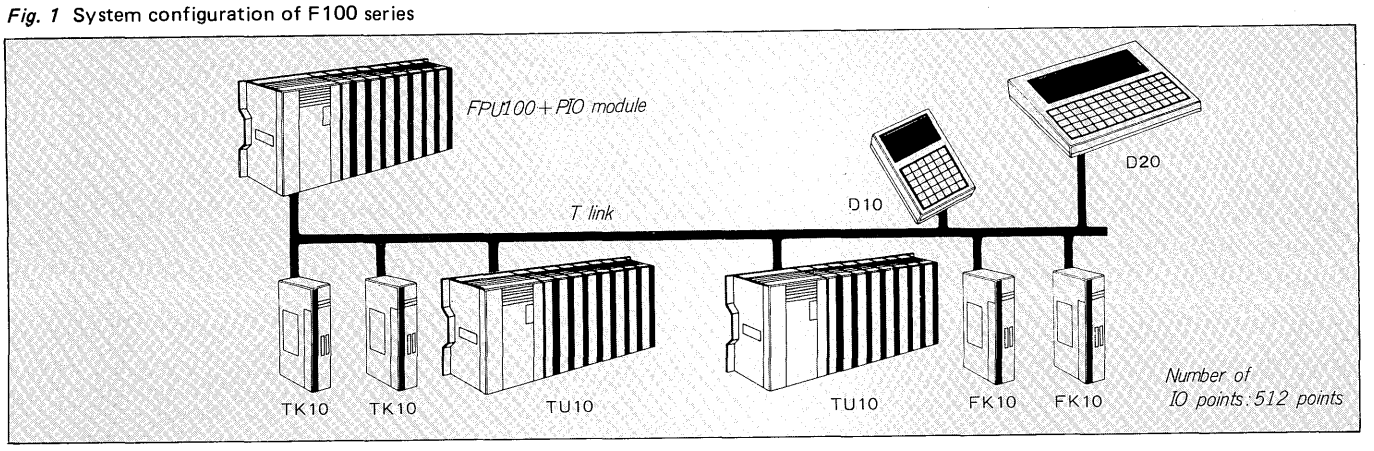


Table 1 Specifications of F100 series

Item			Specifications		Remarks
			FPK100, FPU100	FPK105	
Control system			Stored program system		
Control function			Cyclic operation control		
Commands	Language		Language for control problem (FPL)		F-series Programming Language
	Type		Basic command: 19 sorts, Application command: 44 sorts.		
	Executing speed		Sequence operation: 1 μs/command		Representative value
	Numeral operation data form		BCD 8 digits		
Memory	Data unit	Element	IC-RAM		* denotes Memory Cassette system. IC-RAM with battery back-up.
	Program unit	Element	IC-RAM* EP-ROM* Selectable as desired.		
		Capacity	8 k step		
Number of input/output points	Digital I/O		512 points (expansible up to 1,600 points)		
	Analog I/O		100 points		
Internal relay data memory	Auxiliary relay/SR		512 points		
	Retentive relay/SR		512 points		
	Differential relay		512 points		
	Step control relay		100 (100 steps)		
	Special relay		560 points		
	Timer	0.01 sec.	128 points		BCD 8 digits
		0.1 sec.	128 points		
	Counter		32 points		BCD 8 digits
	Word memory		128 words		1 word = 32 bits
	File memory		128 words		1 word = 16 bits
	P link memory		–	2 k words	
T link	No. of links		1		Remote PIO
	No. of connecting capsules		32		
P link	No. of links		–	16	
Types of inputs/outputs			As per standard input/output interface of the F series		
General Specifications			As per basic specifications of the F series		
Dimensions (mm)			FPK100, FPK105: 148.5 (W) x 250 (H) x 97 (D) FPU100: 482 (W) x 250 (H) x 100 (D)		

numerical value operation command and file processing command are executed by CPU firware. Bit processors, transmission LSI in interface with T link, and P link processor in interface with P link are all controlled by CPU firmware.

The following description gives the outline of the control functions by firmware.

4.1.1 Initial processing

Initial processing is started by "Start Instruction" and carries out the following processing.

(1) Self-diagnosis on the fundamental hardware unit.
(2) Making out of the control table.
(3) Initial setting of various registers.

4.1.2 Execution of application program

For executing the application program, the bit processor will carry out the sequence control according to the indication of rudder diagram. When the bit processor detects the word processing command, execution of command processing is transferred to CPU, while the command is being detected. While the bit processor is processing the program, CPU will execute starting of transfer LSI, constant-cycle timer processing, RAS processing and others. By adeptly using both processors, even these programs in which sequence processing command and word processing command are found side by side, can be processed efficiently.

4.1.3 Input/output data processing

Input/output data regions in the processor capsule are as-signed 1:1 in accordance with the PIO capsule "prefix" number. Input/output control in the application program may be dispensed with only reading out and writing in this region. Delivery and reception of data with PIO capsule are effectuated in constant cycle by firmware and the transfer of those data to input/output data region is executed in synchronization with the cycle of the application program.

4.1.4 Data management

The standard data form is that of BCD 8 digits, in this way, handling of numerical values are simplified. Further than this, binary integer forms are also possible. Conversion between BCD and binary form can easily be made in the application program.

4.1.5 Self diagnosis

By firmware, the fundamental functions such as bit processors and register read/write check are effectuated in this series, thus effectuating hardware checks.

4.2 Operation

For operations of FPK100/105, and FPU100, two modes are available: Operation Mode and Stop Mode. Switching over of the operation modes is carried out by Switchover Instruction from Program Loader. This eliminates the necessity of providing an operating switch, simplifies the construction and makes remote control possible.

5 HARDWARE

5.1 Composition

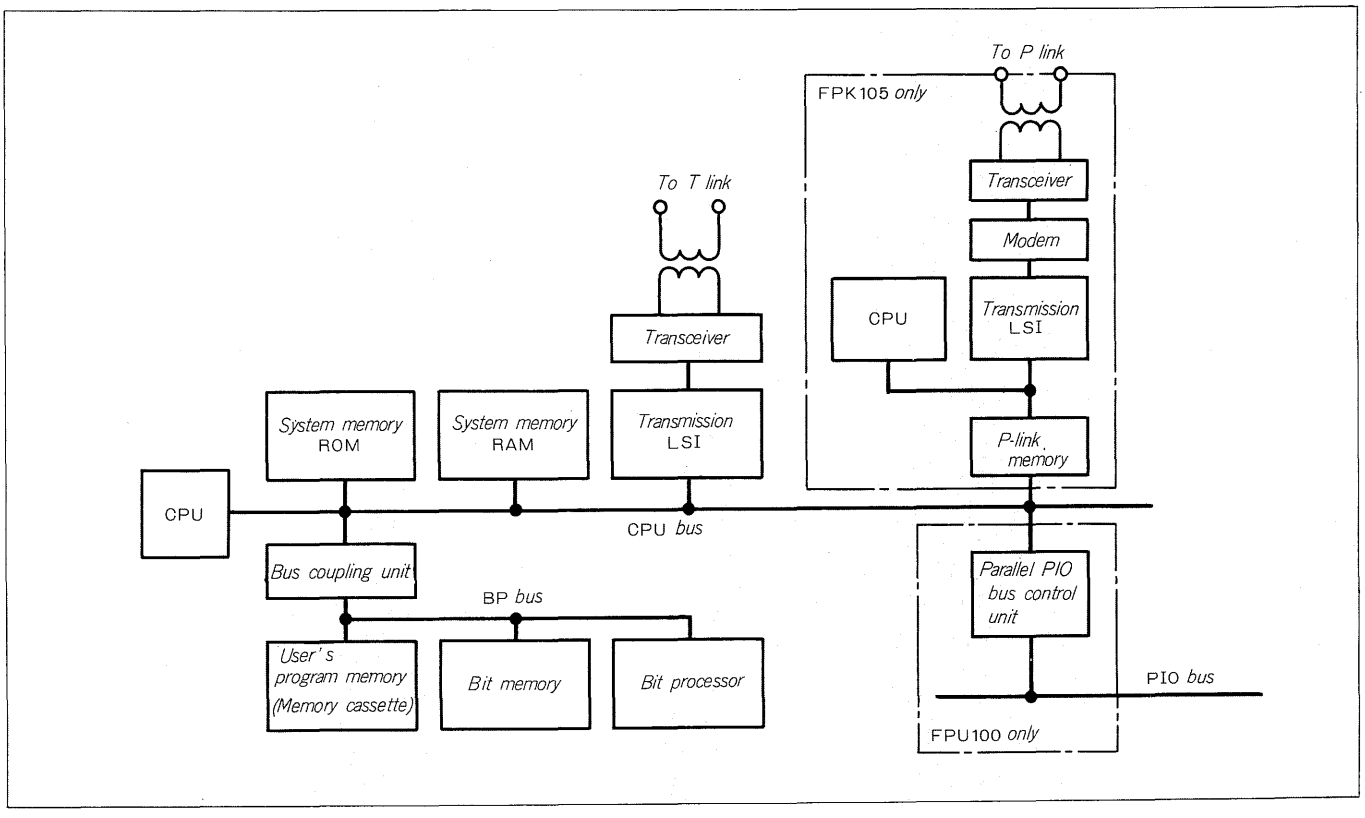
Block diagram of the hardware is as shown in *Fig. 2*. The hardware of this system is composed of CPU, bit processor, T link interface, P link interface, parallel PIO bus interface and various memories, having the following features:

(1) Compact hardware

By adopting LSI of exclusive use and hybrid IC, hardware is simplified and high function is attained in a compact shape.

(2) High-speed processing

Fig. 2 Hardware composition of F100 series



By developing LSI of exclusive use, bit computation processing can be effectuated much in much higher speed and, at the same time, by dividing functions of word processing and bit processing in the processor level, high-speed processing as a whole is attained.

(3) Dispersion installation of PIO

By adopting serial interface in LSI (T links), high-speed and long-distance transmission of PIO data is made possible. A total of 512 input/output point PIO's can be installed on the most convenient spots in a dispersed form as desired.

(4) High-speed inter-processor communication

FPK105 has a P-link interface function, with which a high-speed transmission (5 M bits/sec.) between processor and capsule is possible, and dispersion type control system can easiliy be architectured.

(5) Low power consumption

By adopting LSI's of exclusive use for circuit components, lowering of power consumption is aimed and the

Table 2 List of commands of F100 series

Classification	Designation	Symbol	Classification	Designation	Symbol
Sequence	a contact	—||—	Comparison	>	[>]
	b Contact	—|/|—		≧	[>=]
	Coil	—( )—		=	[=]
	Set	—(S)—		≦	[<=]
	Reset	—(R)—		<	[<]
	Rising edge differential	—(↑)—		≠	[≠]
	Falling edge differential	—(↓)—	Logic Operation	AND	[AND]
	Inverse	—/—		OR	[OR]
	Shift register	SR		EOR	[EOR]
				Inversion	[INV]
				Shift Right Logical	[SRL]
				Shift Left Logical	[SLL]
	Step sequence	Sxx.xx Sxx.xx —||— ( )	Conversion	Binary/BCD	[BCD]
				BCD/binary	[BIN]
Timer	ON delay timer	[TON]		Decode	[DECO]
	OFF delay timer	[TOF]		Encode	[ENCO]
	Integrating timer	S TMR R		7 Segments	[7SEG]
				Count ON-bit	[BCNT]
	Monostable	[MS]	Move	Move	[MOV]
	Monostable (Retriggerable)	[MR]		Move logic	[BT]
Counter	Counter	↑ CTR R		Move digit	[DT]
	Down counter	↓ CTD R		Move upper digit	[MOVU]
				Move lower digit	[MOVL]
	Up-down counter	↑ UDCT ↓ R	Analog	Upper limit	[⊢]
				Lower limit	[⊣]
	Ring counter	↑ RCTR R	File	Store FIFO	[FFST]
				Load FIFO	[FIFO]
				Load LIFO	[FILO]
Arithmetical Operation	Add	[+]		Define file	[FILE]
	Subtract	[−]		File clear	[FLCL]
	Multiply	[×]		Selector	[SEL]
	Divide	[÷]		Deselector	[DSEL]
	Divide (Rounded off)	[÷R]	Program Control	Program entry	[PROG]
	Change sign	[+/−]		Program end	[PEND]
	Increment	[+1]	Branch	Jump	[JMP]
	Decrement	[−1]		Jump end	[JEND]

system is cooled by natural air.

5.2 Exclusive-use LSI's

In this system, hardware constituting the core of the internal control is made LSI of exclusive use, thus improvement of processing speed and perfectioning of functionality are attained.

The following is the outline of the various LSI's adopted.

(1) Bit processor

This is an LSI that carries out directly the instructions of rudder diagram language. This system acquires high processing speed of 1 μs/contact by making bit processor memory access high speed.

(2) T link and P link interfaces

T link interface consists of transfer LSI and hybrid IC for circuit interface of exclusive use. The transfer LSI effectuates DMA for system memory, parallel/serial conversion and modulation/demodulation of transfer data. The hybrid IC is a transceiver for transfer circuit.

P link interface is composed of the same transfer LSI as that of T link interface, hybrid IC and high-speed modem LSI.

6 SOFTWARE

6.1 Program composition

The number of the application program is one, and its execution is processed by cyclic processing system that executes from the beginning to program end command repeatedly

6.2 Commands

Table 2 shows a list of commands that can be used in the F100 Series.

7 CONCLUSION

F100 series is a high-speed PC that executes directly the indication of rudder diagram. This article introduces an outline of composition, specifications, hardware and software of this series.

The main features of F100 series consist in that it has a compact construction and a wide range of command language as well as an inter-processor network and between terminal (PIO) network.

It is much expected that the system would be used widely in the trend of automatization of systems as FA and FMS.

TOPICS

ENGINE GENERATOR FOR PUMPING UP POWER PLANT AT SAMRANGIN, KOREA

The engine generators (2 x 385MVA) that have been delivered to Pump-up Power Plant at Samranjin of Korean Power Supply Co., Ltd. and that have been for some time under installation work have started their exploration towards the end of 1985.

The equipment is of record breaking capacity, next only in capacity to Hermes (448.5MVA) and Bascante (400MVA), and they have magnetic bearings that are patented by Fuji Electric Co., Ltd. This magnetic bearing is intended for reducing the stationary friction torque at the time of pump starting and during the stable running, to reduce the load applied to the thrust bearing, and at the same time, it improves the useful life and reliability of the thrust bearing and enhances the efficiency.

Also, engine generators that have been ordered due to these characteristic techniques and our record, destined to ESCOM Palmiette Pumping Up Power Plant (2 x 250MVA) are under designing and construction without incident.

Rotor in preparation for suspending