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HIGH VOLTAGE DMOS PROCESS TECHNOLOGY

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1. FOREWORD

High voltage monolithic ICs that consist of low voltage control circuits and high voltage devices in one chip are vigorously being developed due to improvements in semiconductor device technology and fabrication process technology. This has created the opportunity for a large decrease in component count resulting in a reduction of system cost and size. In addition, the smaller number of interconnects enhances system reliability.

Against this background, Fuji Electric has developed high voltage DMOSIC technology based on silicon gate CMOSFETs. Using this technology, low voltage logic circuits and DMOSFETs for high voltage circuits can be fabricated on the same chip.

In order to integrate these DMOSFET devices with high voltage bipolar transistors for higher power loads, a new fabrication process technology has been developed. Application has been successful in the field of driver ICs for several kinds of emission displays. In this paper, the unique high voltage DMOS process technology developed by Fuji Electric will be introduced.

2. FEATURES OF THE TECHNOLOGY

2.1 Isolation technology

It is important for each elemental device of a high voltage monolithic IC to be electrically isolated. Therefore, many experiments have been made with regards to this isolation problem, and several methods have been developed, each of which has advantages and disadvantages. The proper isolation method must be selected according to the application. A typical cross sectional structure of a p-n junction isolation (JI) and a dielectric isolation (DI) are shown in *Fig. 1*.

DI structure realizes a lesser parasitic effect and needs less space than JI structure. However, JI structure is superior to DI structure in terms of production costs, manufacturing and minute processes. Fuji Electric has selected p-n junction isolation structure mainly because of low production costs.

Fig. 1 Isolation technology

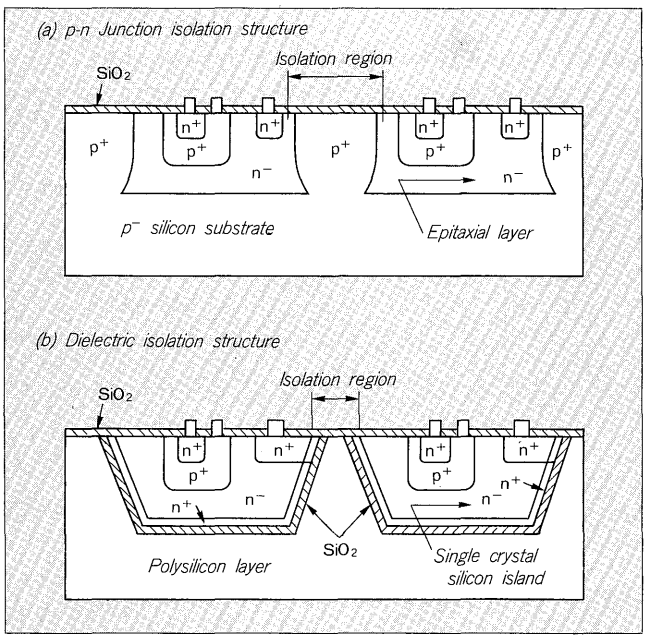
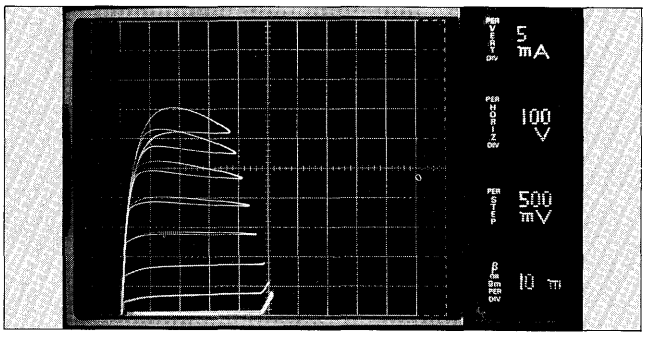


Fig. 2 I-V characteristics of 400V class high voltage n-channel DMOSFET



As for the parasitic effect, when JI is selected the problem is solved by understanding the relationship of the potential between each area.

In the 200 V class process, development has been completed and the technology has been applied to several products. New 400 V class isolation technique is currently

Fig. 3 The closs-section of high voltage DMOSIC

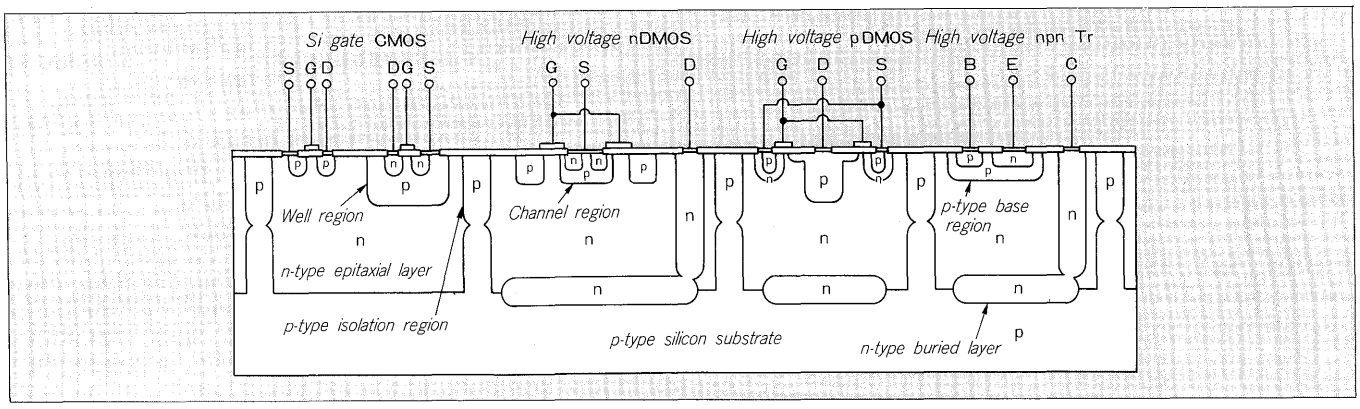
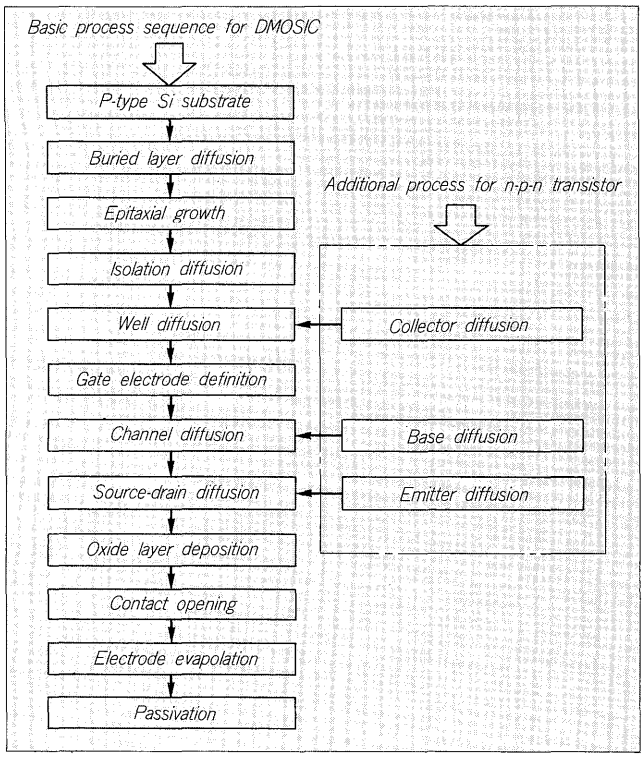


Fig. 4 The outline of high voltage DMOSIC process



being developed using a new junction isolation structure. The output characteristics of a high voltage n-channel DMOSFET which has a blocking capability of 450 V are shown in *Fig. 2*.

2-2 Elemental devices and fabrication process

The cross-section of a DMOSIC and an outline of its fabrication process are shown in *Figs. 3* and *4*, respectively. Low voltage logic circuits and high voltage n-channel, p-channel DMOSFETs are constructed on the same epitaxal wafer using p-n junction technology as described above. In the low voltage logic circuits, silicon gate CMOSFETs are used, which are suitable for realizing low power dissipation and high speed operation. The high voltage DMOSFETs are suitable for high voltage operation. In addition, high voltage n-p-n transistors which are used for higher power output instead of DMOSFETs can also be made with the same process sequence. As a result, this unique fabrication process technology has been realized, which can integrate many kinds of devices for many different purposes.

High voltage n-channel DMOSFETs and n-p-n Transistors have structures which result in vertical current flow and high voltage p-channel DMOSFETs are designed to have lateral current flow.

Poly-silicon is used at the gate electrodes of each MOS device and for high voltage MOSFETs, the source and channel are constructed by DSA (Diffused Self Alignment) technique. Using this technique, highly doped short channel can easily be obtained. This structure allows the depletion region to extend into the drain region without extending into the channel region. This characteristic prevents punch-through from occurring. In addition, by improving the mask patterns and controlling the impurity density, the intensity of the electric field in each device is reduced and as a result, high voltage ICs are realized. To protect against parasitic MOS effects due to interconnection, diffusions for channel stopping and field plates are used.

2-3 Characteristics of elemental devices

Low voltage logic consists of silicon gate CMOSFETs and has the following geatures.

(1) Power supply : 5-15 V
(2) Power dissipation : 10 mW (5 V, 4 MHz)
(3) Maximum clock frequency : 10 MHz

Next, the characteristics of the high voltage devices which are responsible for the high voltage part will be discussed. The output characteristics of high voltage n-channel and p-channel DMOSFETs are shown in *Fig. 5*, and *6*, respectively. N-channel DMOSFET has a voltage capability of 230 V and on resistance of 400 ohm. P-channel DMOSFET has a blocking voltage of 250 V and an on resistance of 2 kohm. The FETs for the output circuit can be properly designed according to the requirements of the application. When large current is required, n-channel MOSFETs of the multi-source type are adopted to reduce the device size. This is shown in *Fig. 7*.

On the other hand, bipolar transistors have the capa-

Fig. 5 I-V characteristics of high voltage n-channel DMOSFET

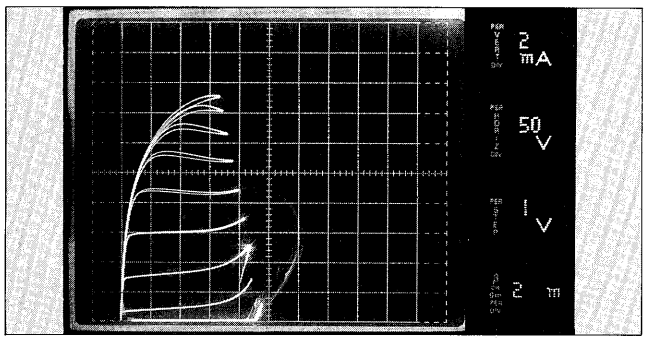


Fig. 6 I-V characteristics of high voltage p-channel DMOSFET

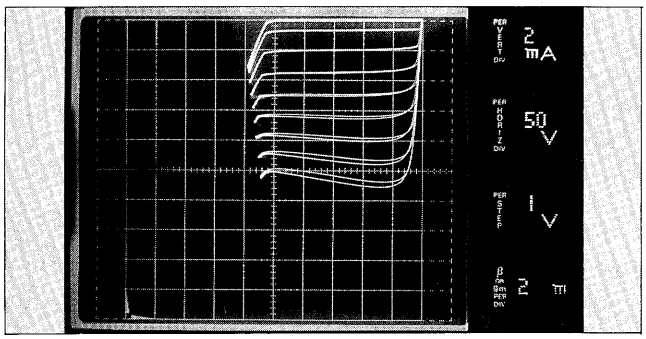


Fig. 7 The structure of multi-source type high voltage n-channel DMOSFET

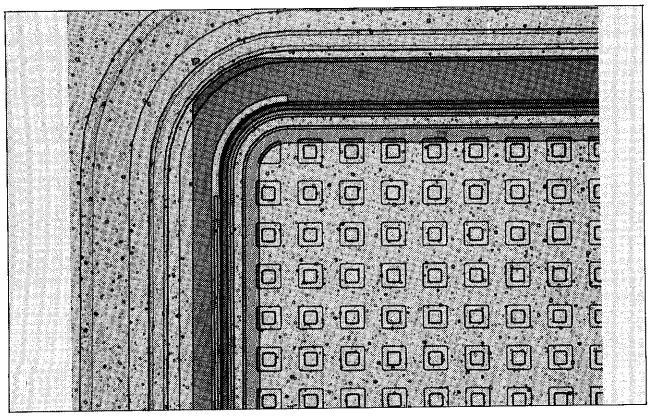


Fig. 8 I-V characteristics of high voltage n-p-n transistor

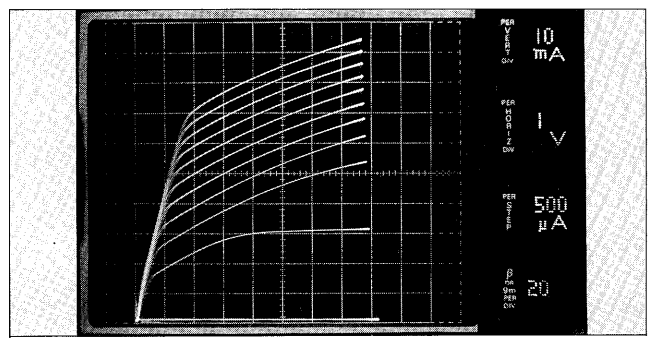


Fig. 9 The blocking capability of high voltage n-p-n transistor

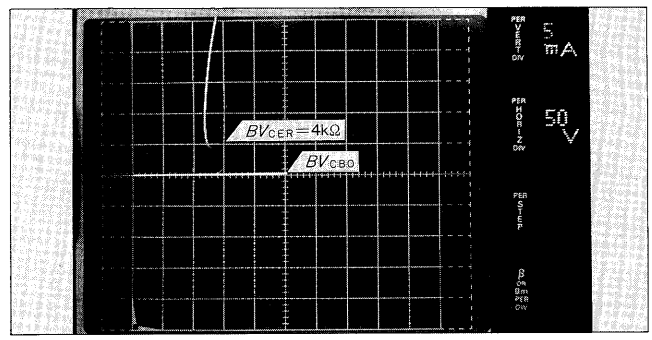
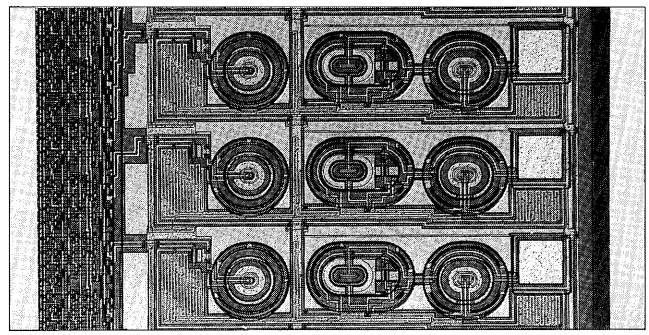


Fig. 10 Push-pull output circuits



bility of controlling larger current than DMOSFETs. The output characteristics of a standard size high voltage n-p-n transistor is shown in *Fig. 8.* On resistance at the saturation region is 25 ohm and it has about a 10-time larger driving capability than an n-channel DMOSFET.

Its blocking capability is shown in *Fig. 9.* By using proper base driving circuits and reducing the resistance between the base and emitter, higher blocking capability has been obtained. The blocking capability between the emitter and collector is shown in *Fig. 9* when the emitter and base are connected with a 4 kohm resistance.

3. APPLICATION CIRCUITS TECHNOLOGY

Several kinds of output circuits which have been applied to DMOSICs are introduced below.

3-1 Level shifting circuits and push-pull output circuits

Push-pull output circuits are shown in *Fig. 10.* A 5V logic signal is translated to the high voltage level by a level shifting circuit which consists of resistors, FETs, and zenner diodes, and from this 200V class output voltage can be obtained.

3.2 Open collector, open drain output circuits

Open collector output circuits in which high voltage n-p-n transistors are connected in a darlington configuration are shown in *Fig. 11.* When the base current is supplied by a 5V CMOS circuit, these transistors drive a 220mA output current.

Open drain output circuits which include high voltage p-channel DMOSFET's are described in *Fig. 12.* Because MOSFETs are voltage-driven devices, they have the good feature of low power dissipation.

Fig. 11 Open collector output circuits

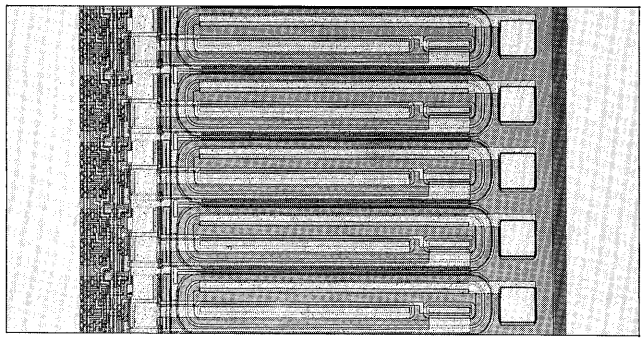
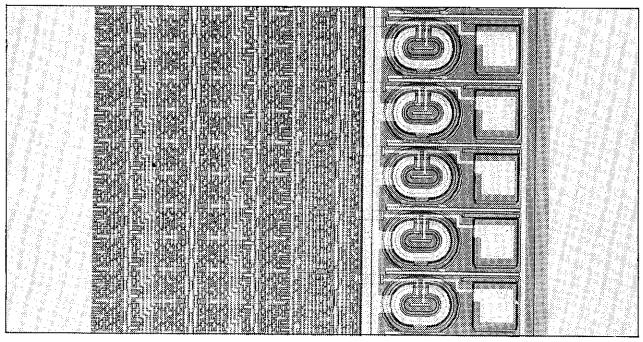


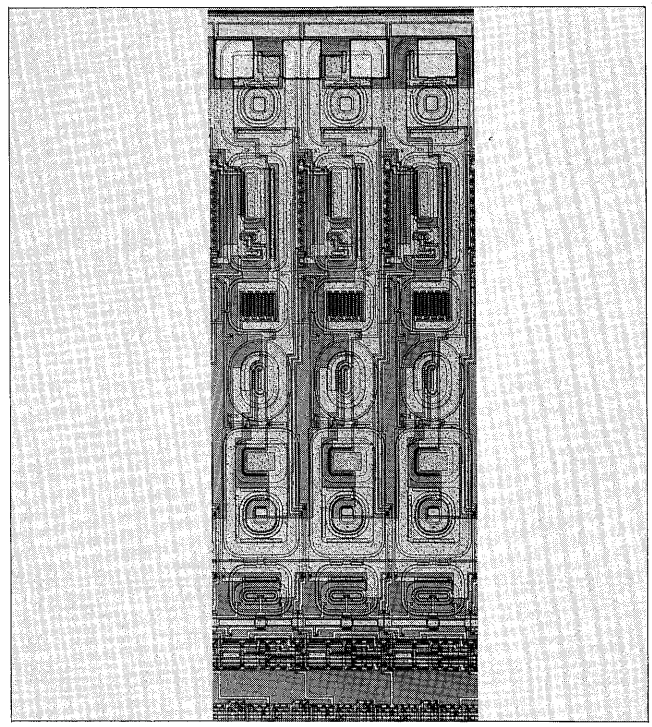
Fig. 12 Open drain output circuits



3-3 High voltage, high current output circuits

As described above, this process technology can realize many kinds of elemental devices on the same chip. The new drive circuits are shown in *Fig. 13*, which use n-p-n transistors as output devices and n-, p-channel DMOSFETs, diodes, and resistors as pre-drive circuits.

Fig. 13 High voltage, high current output circuits



4. CONCLUSION

A high voltage DMOS process technology has been developed which combines not only DMOSFETs but also high voltage n-p-n transistors with low voltage control circuits on a single chip. Further, the most efficient designing techniques have been established.

This technology has resulted in a wide variety of new applications.

Advanced process technology and improved device structures for 400V and above are now being developed, and new applications are being found in which this new technology can be used.