800 V Class HVIC Technology

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ABSTRACT

To help achieve energy savings in the power systems at IDC (internet data center), 800 V guaranteed HVIC (high voltage IC) technology has been established. A proprietary device process based on self-isolation was developed. To realize energy savings in a power system, the switching efficiency of the bridge circuit used in the power system must be improved. To achieve this improvement, component and circuit technology capable of reducing the I/O propagation delay of ICs to less than 100 ns was developed. Additionally, technology for guaranteeing the ability of a HVIC to withstand the essential high dV/dt and negative voltage surges was also established.

1. Introduction

In the span of six years from 2006 through 2011 in the United States, the total power consumption of IDCs (internet data centers) has nearly doubled, which is an increase comparable to the amount of power that could be supplied by the construction of 10 new nuclear power plants.

In Japan, by 2025, the amount of information that flows through the Internet is expected to be about 200 times that of 2008, and the power consumption by IDCs will reach approximation 2.5 times the amount of 2008. Moreover, the total power consumption by ICT (information and communication technology) devices, which accounts for approximately 5% of the total power consumption in Japan in 2006, is predicted to reach approximately 20% by 2025. Initiatives to realize energy savings and higher efficiency of IDCs are an important part of the efforts to prevent global warming.

To contribute to energy savings at IDCs, Fuji Electric has developed 800 V-class HVIC (high voltage IC) technology for realizing higher efficiency, lower energy consumption, smaller size and higher reliability of IDC power supply equipment such as servers, UPSs (uninterruptible power supplies) and the like. In the development of this technology, Fuji Electric has established proprietary device process technology based upon a low-cost self-isolation process. Moreover, in order to realize energy savings in power supply systems, improvement is needed in the switching efficiency of the bridge circuit that configures the power supply system, and to realize this, Fuji Electric has also developed circuit element technology capable of limiting the I/O propagation delay time to less than 100 ns. Additionally, Fuji Electric has also established technology for ensuring the necessary high dV/dt tolerance in an HVIC. This paper introduces this device process technology and circuit element technology.

2. Features of 800 V Class HVIC Technology

An HVIC is a high voltage IC that drives the gates of power devices arranged in a bridge circuit configuration. The intermediate potential of upper arm and lower arm power devices rises to a high potential of several hundred volts during switching of the upper arm power device, and therefore HVICs are required to be able to withstand high voltages. Moreover, compared to a conventional drive system using an optocoupler or pulse transformer, a drive system that uses a HVIC will be able to realize power supply systems that are smaller in size and more highly efficient. Fig. 1 shows

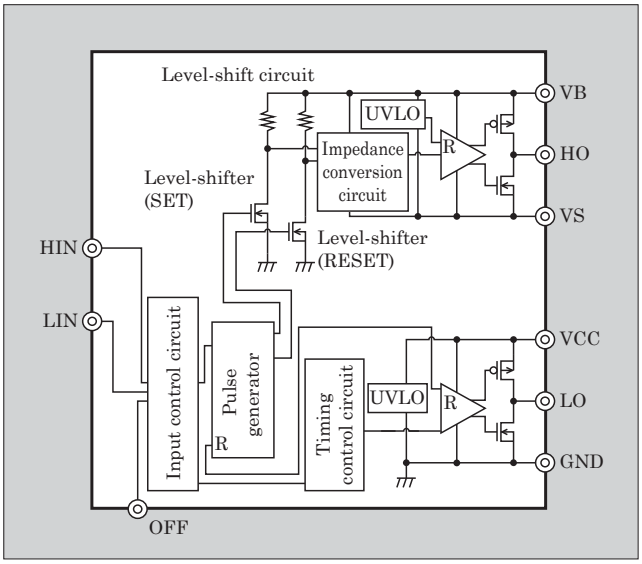

Fig.1 HVIC circuit block diagram

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a block diagram of the HVIC circuit that has been developed. The HVIC is equipped with high-side and low-side drive circuits, level-shift circuit, an impedance conversion circuit, an UVLO (under voltage lock out) circuit, an input control circuit and so on.

Fig. 2 shows a self-isolation type 800 V -class HVIC chip prototype that was built for 200 V AC power supply equipment.

Features of the HVIC are listed below.

(a) Guaranteed 800 V class performance, high-side circuit power supply voltage of 30 V
(b) High-side turn on/off propagation delay time of less than 100 ns
(c) Wire bonding level-shift that applies HV wiring technology
(d) Guaranteed high negative voltage surge tolerance and dV/dt tolerance (≥50 kV/μs)

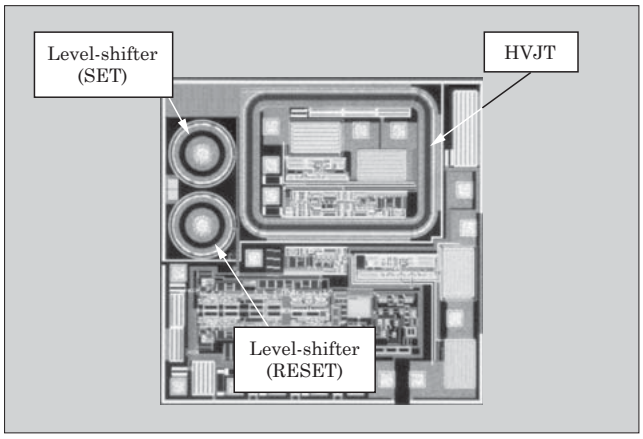

Fig.2 Self-isolation type 800 V class HVIC prototype chip

Table 1 List of 800 V class HVIC device elements

Category	Name	Intended use
Active element	7 V class LV gate low voltage n-MOSFET	Pulse generator, etc.
	7 V class LV gate low voltage p-MOSFET	
	30 V class LV gate intermediate voltage n-MOSFET	High-side and low-side output stage drivers, UVLO, latch circuit logic
	30 V class HV gate intermediate voltage p-MOSFET	
	30 V class HV gate intermediate voltage n-MOSFET	
	800 V class HVNMOSFET for level shifting	Level shift device
	30 V class NPN BJT	Internal power supply circuits, etc.
	30 V class NPN BJT	
	30 V class diode for ESD protection	ESD protection circuits, etc.
	5 V/7 V class Zener diode	
Passive element	High-resistance poly-silicon resistance	Impedance conversion circuit, etc.
	Low temperature compensation poly-silicon resistance	
	MOS capacitance	Noise filter, etc.
	Poly-silicon capacitance	

Moreover, the developed HVIC is an 800 V class device, and therefore compared to a 600 V class HVIC[1], when a lightning surge enters the power supply system or when used in a harsh power supply environment and noise is generated, there is the benefit in that the IC will not incur damage before the 600 V class power devices such as IGBTs (insulated gate bipolar transistors) and MOSFETs (metal-oxide-semiconductor field-effect transistors).

3. Device and Process Technology

Isolation methods for the elements that form power ICs include self-isolation, pn junction isolation and dielectric isolation. In a dielectric type HVIC, a buried oxide layer exists between the substrate and the active layer on which high-side devices and level-shift elements are formed, and as a result, this device has a smaller junction capacitance than either the self-isolation type or pn junction isolation type of IC, and is suited for high-speed performance. An additional benefit is that parasitic device malfunction and latch-up caused by negative voltage surges or the like are less likely to occur with dielectric type HVICs. However, the dielectric type HVICs presently on the market are at most 600 V class devices, and 800 V class or higher performance is technically extremely difficult to realize[2]. On the other hand, self-isolation type HVICs require a larger element isolation area, but have the advantages of easily increasing their breakdown voltage and of having a less expensive substrate cost.

Table 1 shows a list of 800 V class HVIC device elements. Since 30 V class intermediate voltage MOSFETs are provided as high-side devices, power device gate drive voltages can be supported over a wide range of up to 30 V. Moreover, ESD (electrostatic discharge) protection diode is ESD protection device having low-avalanche resistance and was developed to protect

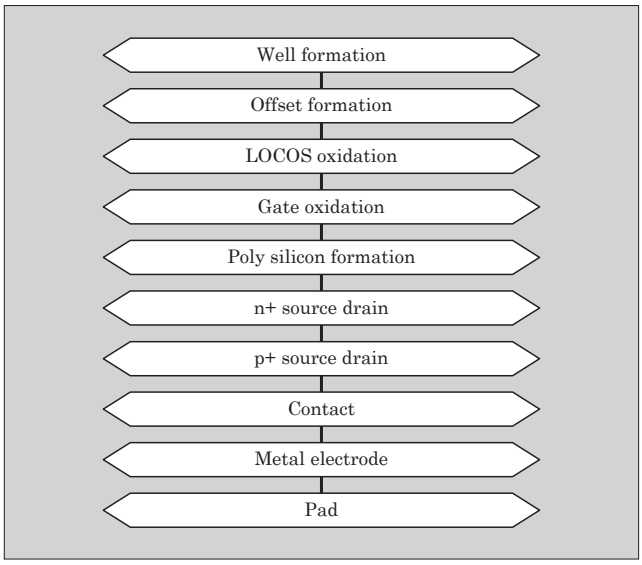

Fig.3 Process flow

the I/O pins of the IC from ESD surges at the time of package assembly and from switching noise applied to the power supply board.

3.1 Process flow

For 800 V class HVICs, the self-isolation method of Fuji Electric's high-voltage BiCMOS (bipolar CMOS) process is used. Fig. 3 shows the process flow. In this process, to form a high-voltage triple well structure provided with a deep diffused layer in the high-side drive circuit region, diffusion is performed at a high temperature for a long time during the well formation process. Additionally, process sharing among devices is being promoted to lessen the labor involved.

3.2 High-side triple well device

The design concept of the 800 V class self-isolation type devices is to use a self-isolation process to realize high tolerance against parasitic malfunction and breakdown, comparable to that of a pn junction isolation type device. A high-side triple well device was developed based upon Fuji Electric's existing high voltage processes.

Fig. 4 shows the cross-sectional structure of high-side and low-side logic devices formed on a p-type substrate (Psub). Between the high-side logic part and the low-side logic part is provided a HVJT (high voltage junction termination) region having a structure that terminates the junction between ground potential and 800 V potential. Moreover, the high-side triple well region, must be designed such that when the potential of the n-type diffusion layer (N2 diffusion layer) of Fig. 4 rises to 800 V, the depletion region extending from the junction between Psub and the N2 diffusion layer does not contact the depletion region extending from the junction between the N2 diffusion layer, which is reverse-biased to the high-side power supply voltage of 30 V, and the p-type diffusion layer (P2 diffusion layer), i.e., there will be no punch-through.

As shown in Fig. 5, the relationship between vertical direction punch-through voltage V_p and the net charge Q_n (value of P2 diffusion layer impurity concentration subtracted from N2 diffusion layer impurity concentration) of the N2 diffusion layer in a high-side

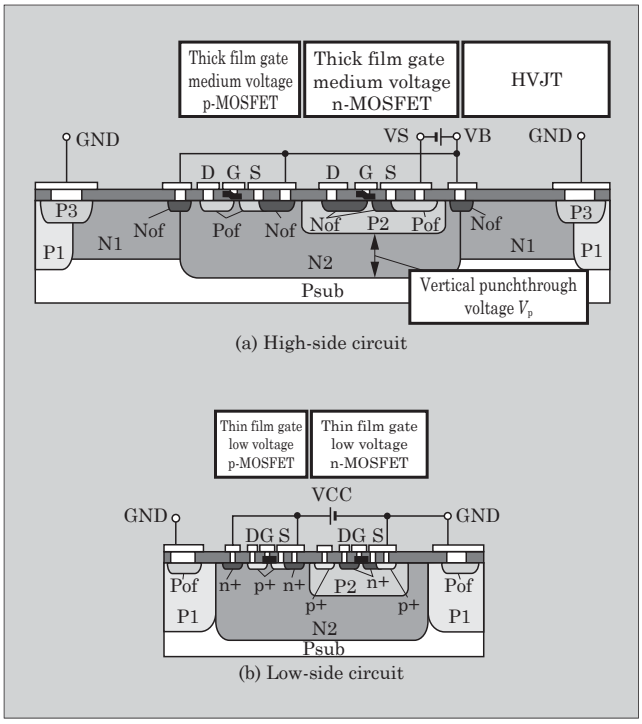

Fig.4 Cross-sectional structure of high-side and low-side logic

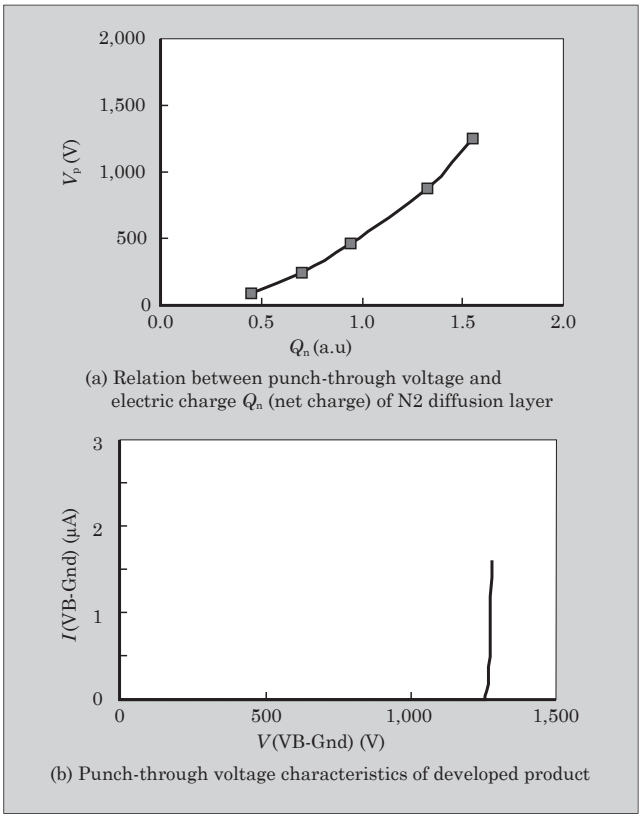

Fig.5 Relationship between vertical punchthrough voltage V_p and high-side triple well N2 diffusion layer net charge Q_n and breakdown voltage characteristics of developed product

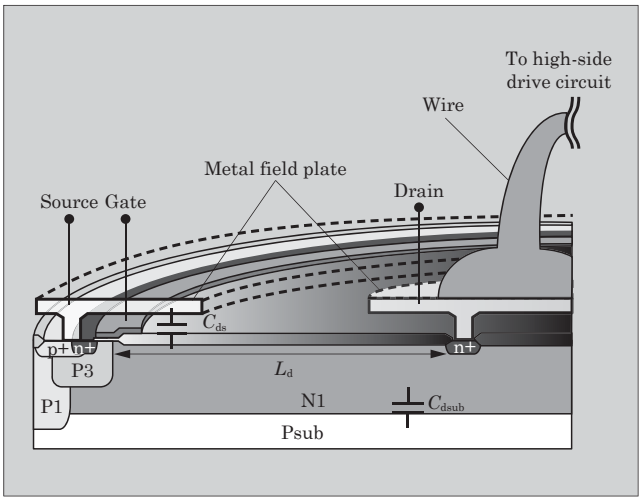

Fig.6 Cross-section of HVNMOSFET used as level shifter

triple well structure consisting of a P2 diffusion layer, a N2 diffusion layer and Psub was clarified using analysis formulas. In this design, the impurity concentrations and diffusion depths of the N2 diffusion layer and P2 diffusion layer are adjusted, and the Q_n value is adjusted so as to ensure breakdown voltage tolerance of at least 1,200 volts.

3.3 800 V class HVNMOSFET for level shifters

Fig. 6 shows the cross-sectional structure of a HVNMOSFET (high voltage n-MOSFET) used as the level shifter of Fig. 1. The SET input side and the RESET input side have the same device structure, and the HV-level shifting interconnection to the high-side drive circuit is implemented with gold wire bonding. In order to realize an 800 V class HVIC, the HVNMOSFET was devised to achieve: (1) 800 V class on-state/off-state breakdown voltage, (2) low parasitic capacitance, (3) high tolerance to parasitic action breakdown and (4) high reliability. Details are described below.

(1) 800 V class on-state and off-state breakdown voltage

By optimizing the concentration and drift region length L_d of the N1 diffusion layer, i.e., the diffusion layer shown in Fig. 6, breakdown voltages of at least 830 V could be achieved in both the on-state (V_g=5 V) and the off-state (V_g=0 V). (See Fig. 7.)

(2) Low parasitic capacitance

Among the parasitic capacitances of the HVNMOSFET, the value of C_{dsub} is determined by the necessary area of the voltage breakdown structure. C_{ds} depends on the metal field plate pattern of the source-side. Adjusting the field plate length on the source side contributed to a reduction of C_{ds} and a shorter high-side propagation delay time.

(3) High tolerance for parasitic action breakdown

Because ESD surges and dV/dt noise entering the reference potential pin of the HVIC are also applied to the drain of the HVNMOSFET, the avalanche resistance of the HVNMOSFET itself must be improved and parasitic action due to displacement current must be suppressed. The pickup structure of the source layer and base layer of the HVNMOSFET has been innovated, and ESD tolerance that sufficiently satisfies the standards, and dV/dt resistance of 50 kV/μs or above at the high temperature of 150 °C has been ensured.

(4) High reliability

The field plate structure between the source and drain of the HVNMOSFET has been optimized to limit the effects of molding compound mobile ions and

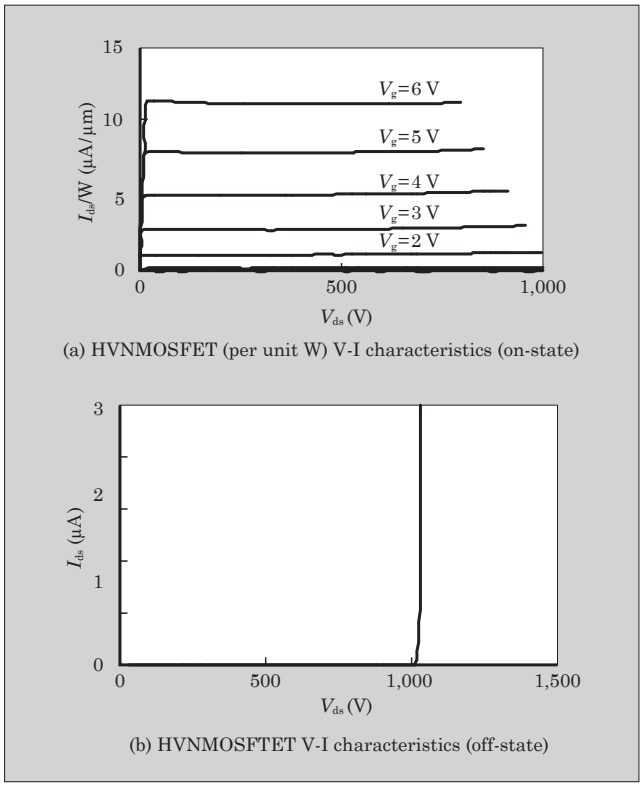

Fig.7 V-I characteristics of HVNMOSFET

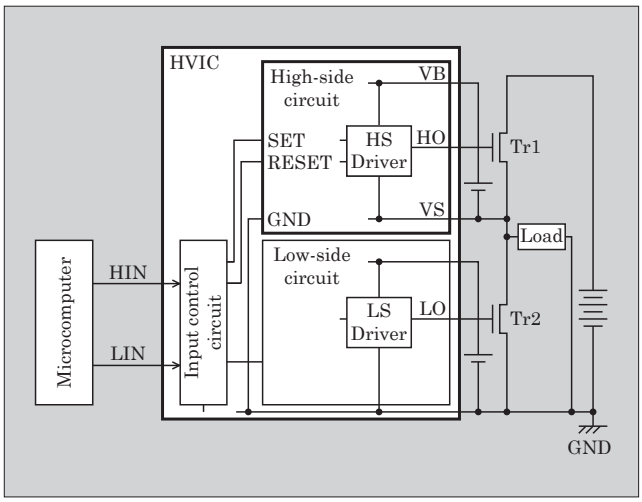

Fig.8 HVIC application example

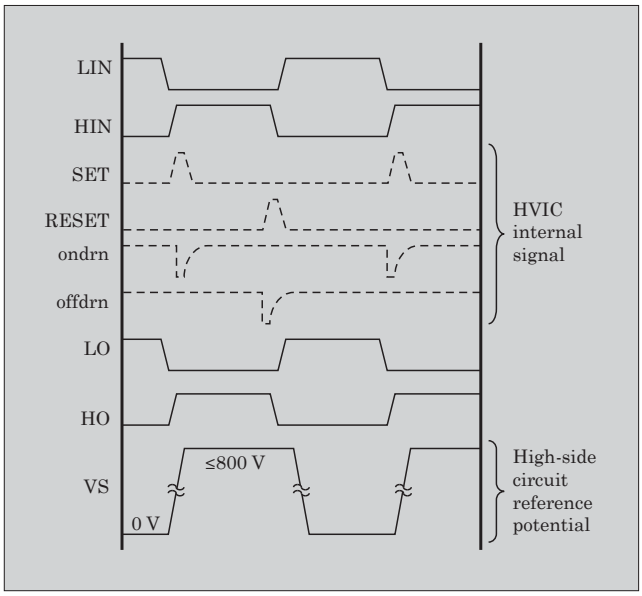

Fig.9 HIVC operation timing chart

hygroscopy on the breakdown characteristics, and high temperature bias tests, high temperature high humidity bias tests, and the like have been conducted to ensure that long-term reliability requirements are satisfied.

4. Circuit Element Technology

4.1 HVIC operation

Fig. 8 shows an example application of the HVIC. The input pins HIN and LIN of the HVIC connect to a microcomputer or the like operating at low voltage, and the output pins HO and LO connect to gate pins of an IGBT or MOSFET in a half-bridge configuration. Fig. 9 shows a timing chart of the HVIC operation. At an input control circuit, the high-side control signal HIN is converted, based upon its rising and falling edges, into the SET and RESET signals and is inputted to the high-side circuit block. Meanwhile, the low-side control signal LIN passes through an input control circuit and is input directly to the low-side circuit block.

For the high-side circuit, the output node of the half-bridge circuit is taken as the V_s reference potential. Because the V_s reference potential fluctuates between 0 and 800 V (max.) due to the alternating on-off operation of Tr1 and Tr2, dV/dt resistance to rapid rising and falling of the V_s potential and resistance to undershoot (negative voltage surge) are requested. Additionally, in order to perform highly efficient power control, reduced retardation time is being requested from the market.

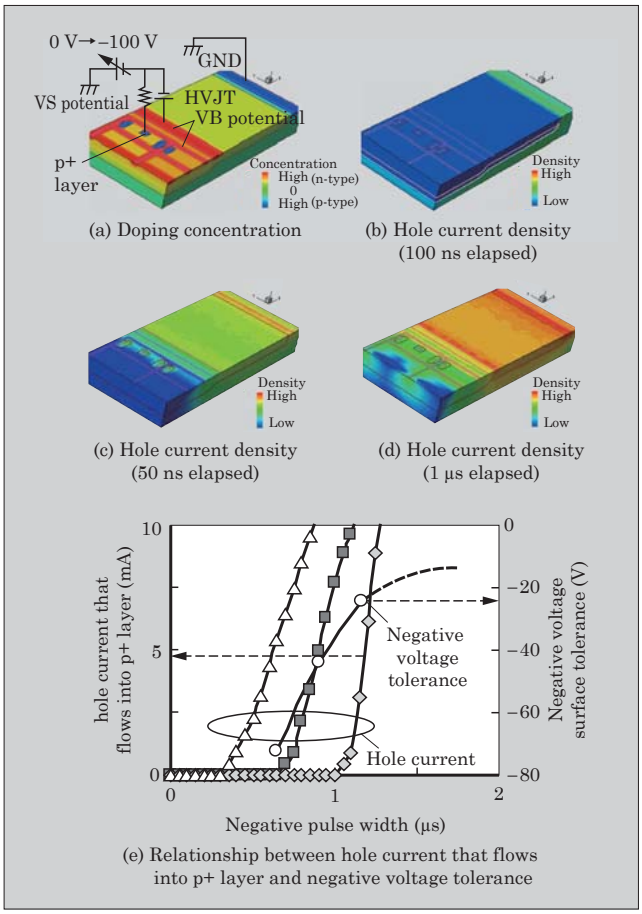

Fig.10 Example transient simulation at time of negative surge voltage generation

4.2 Negative voltage surge resistant layout design technique

As described above, the instant that the upper arm of a power device is turned off, the induced electromotive force of the load causes the V_s reference potential of the HVIC to drop several tens of volts below the reference value for a duration of several hundreds of nanoseconds. The density of the hole current that flows into the high-side circuit when the V_s reference potential is in a negative voltage state is shown in Fig. 10. Using three-dimensional transient simulations, the relationship between negative voltage pulse width and negative voltage surge resistance is quantified and reflected in the layout design.

4.3 Characteristics of high-side drive circuit

Fig. 11 shows an internal block diagram of the high-side circuit. The high-side circuit is configured from three blocks: a level-shift circuit block, a latch circuit block and a driver circuit block. The basic configuration of the level shift circuit combines resistive devices LSRs and LSRr, HVNMOSFET (SET) and HVNMOSFET (RESET) to form a common-source amplifier. To prevent malfunctions caused by fluctuation in the

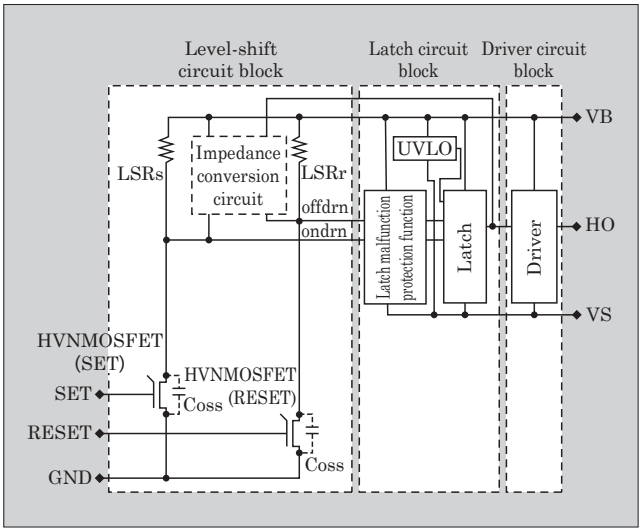

Fig.11 Internal block diagram of high-side circuit

Table 2 Function table of latch malfunction protection function

Input		Latch output
SET (offdrn)	RESET (ondrn)	
L	L	Hold
H	L	H
L	H	L
H	H	Hold

reference voltage level between 0 and 800 V (max.), an impedance conversion circuit has been devised.

The latch circuit, as shown in Table 2, is provided with a latch malfunction protection function for retaining the latch output when the SET side and RESET side signal statuses are both in the same logic state.

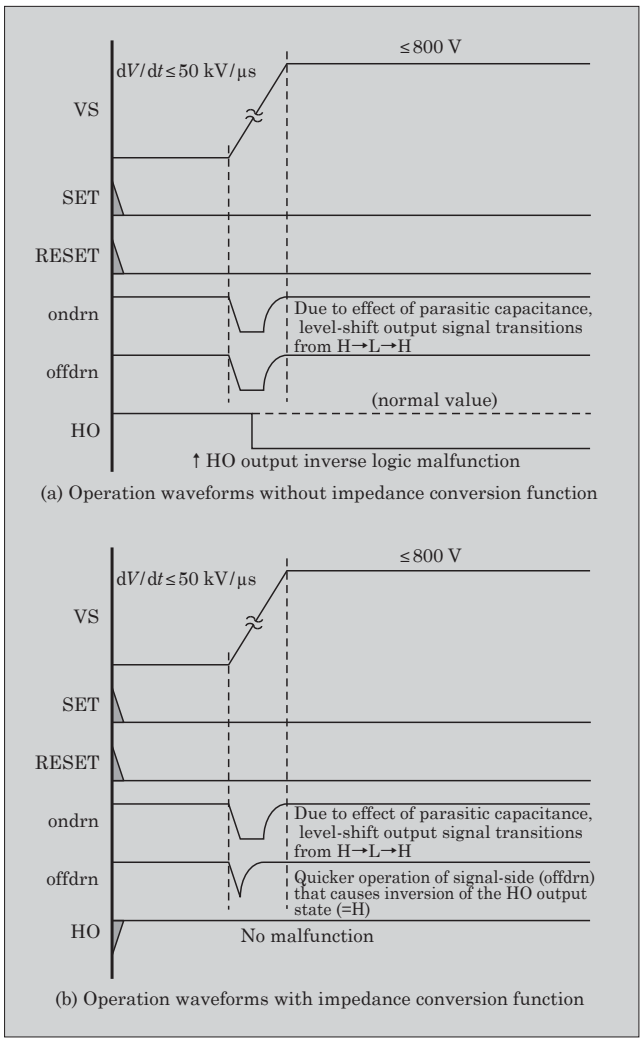

Fig.12 Operation time charts of high-side circuit when d*V*/d*t* is generated

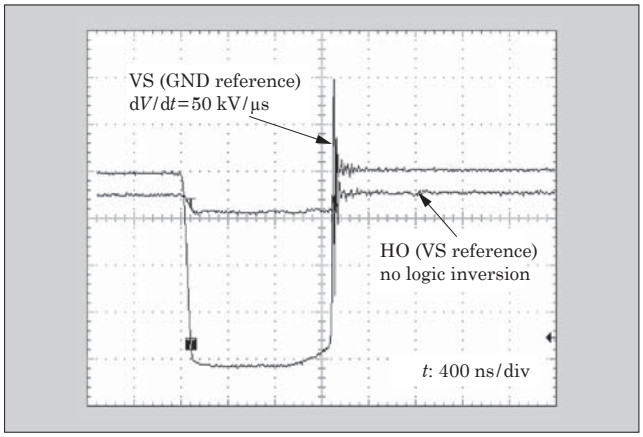

Fig.13 Measured waveforms when d*V*/d*t*=50 kV/μs

In addition, a low pass filter is provided for protecting against erroneous output when the logic level changes instantaneously due to d*V*/d*t* generation or the like. The drive circuit uses the push-pull drive method and is configured from MOSFETs having the drive capacity and dimensions that satisfy market requests for performance and the like.

4.4 d*V*/d*t* tolerance

Fig. 12 shows timing charts of the operation of the high-side drive circuit when d*V*/d*t* is generated. Fig. 12(a) shows the output states of the level-shift circuit in the case where there is no impedance conversion function. Even if the HIN input is at a low-level, the generation of d*V*/d*t* causes the V_s reference potential to fluctuate due to parasitic capacitance of the HVNMOSFET and the d*V*/d*t*, thus generating a current flow. As a result of this current, the HVNMOSFET drain on the SET-side and RESET-side is charged and discharged and the level-shift output changes from high to low to high. As a result, the HO output is susceptible to inverse logic malfunctions. Therefore, to prevent inversion malfunctions, the high-side circuit is provided with an impedance conversion function enabling the operation shown in Fig. 12(b).

Fig. 13 shows the measured waveform when d*V*/d*t*=50 kV/ms and Table 3 lists the measured results of the temperature characteristic of the d*V*/d*t* tolerance. With the impedance conversion function, inverse logic malfunctions of the HO output were found to be prevented even when d*V*/d*t* of 50 kV/μs was generated. In addition, it was also confirmed that inverse logic malfunctions do not occur in the temperature range of −40 °C to +150 °C.

Table 3 Measured results of d*V*/d*t* tolerance in voltage range of VB=0 to 30 V

	Temperature (°C)			
	−40	25	125	150
d*V*/d*t* tolerance DC to 50 (kV/μs)	○	○	○	○

○: Inverse logic behavior does not occur

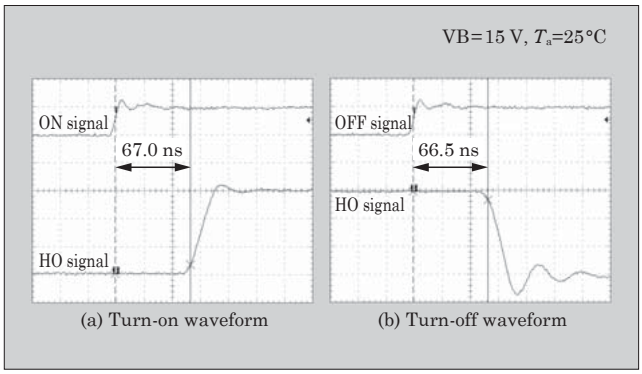

Fig.14 Measured results of turn-on and turn-off delay times

4.5 Delay time characteristics

Fig. 14 shows delay time waveforms of the high-side circuit. Fig. 14(a) shows the turn-on delay characteristics, and Fig. 14(b) shows the turn-off delay characteristics. In the voltage range of VB = 9 to 30 V, delay times of less than 100 ns were achieved.

5. Postscript

In this paper, the device, process and circuit elements technology of a newly developed 800 V class HVIC for power supply use have been introduced.

This technology not only realizes high reliability of the IC in terms of 800 V class performance and high surge tolerance, high dV/dt tolerance and the like, but through reducing the propagation time delay to less than 100 ns, also contributes to the higher efficiency, smaller size and lower cost of power supply systems. In the future, Fuji Electric intends to deploy this technology horizontally in the industrial sector consisting of general-purpose inverters, IPMs (Intelligent Power Modules) and the like, the consumer sector consisting of air conditioners, lighting and the like, and automotive sector consisting of the HID (high intensity discharge lamp) and the like.

References

(1) T.Yamazaki, et al, New High Voltage Integrated Circuits using Self-shielding Technique. Proceedings of the 11th ISPSD. 1999, p.333-336.

(2) M.Yamaji, et al, A Novel 600 V-LDMOS with HV-Interconnection for HVIC on Thick SOI. Proceedings of the 22th ISPSD. 2010, p.101-104.