U-series IGBT Modules (1,700 V)

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1. Introduction

In recent years, requirements have increased for high voltage power semiconductor devices used in high voltage power converters such as industrial inverters. The IGBT (insulated gate bipolar transistor), which has a high switching speed, low power dissipation loss and high voltage capability, has been replacing the conventionally used GTO (gate turn-off thyristor) and SCR. Advances in a comprehensive technological approach to IGBT design, including device design, process design and application design, have driven new IGBT development. The favorable response to market demands for economy and reliability serves to further promote the reputation of the IGBT.

Fuji Electric has recently developed a 1,700 V U-series IGBT in order to meet demands for larger current, smaller size and higher reliability. A trench structure is formed on the front surface and an FS (field stop) structure is formed on the back in order to achieve an improvement in the overall power loss. By optimizing characteristics of both structures, Fuji Electric succeeded in developing an IGBT that has very low power loss. In developing a highly responsive and low-loss IGBT, it was also necessary to improve characteristics of the FWD (free wheeling diode) . The IGBT and FWD should be thought of as a single integrated unit. Fuji Electric has developed a FWD with soft recovery characteristics for noise reduction. This paper introduces the device characteristics and the product series of U-series IGBT modules.

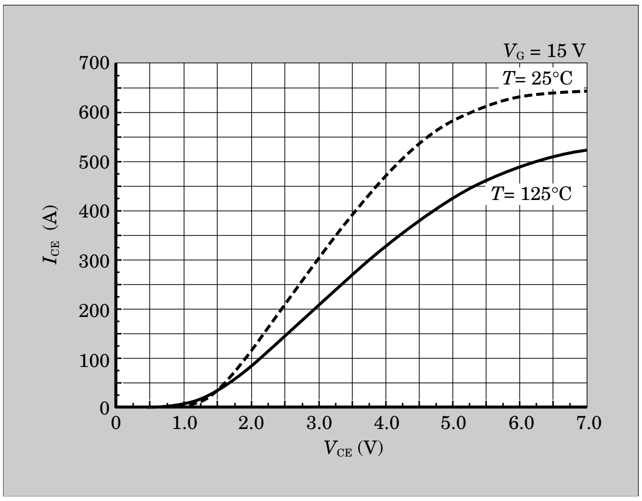
2. Characteristics of the New IGBT

The surface of a conventional IGBT has a planer structure, therefore,its cell density is low and $V_{CE\ (sat)}$ is degraded by the J_{FET} resistance of this surface. Moreover, the NPT structure of the wafer substrate resulted in a thick wafer with a poor $V_{CE\ (sat)}$-E_{off} tradeoff characteristic. The rated current density of the newly developed 1,700 V IGBT is set to over 130 A/cm^2, and the key development was increasing base current in the wide base transistor built into the IGBT. To optimize the surface structure, we run simulations for front surface and back surface structures. Based on the results, we applied a trench structure to the surface. The trench structure eliminates J_{FET} resistance on the surface of the planer structure. Accompanying the increase in cell density, the electronic current from the surface increases, and a sufficient base current can be secured. Increasing the percentage of electron current among the total current enables turn off switching loss to be decreased.

Next, to achieve further improvement in the characteristics, we developed an FS structure and applied this structure to the IGBT. By applying the FS structure, resistance of the substrate wafer decreased, enabling both $V_{CE\ (sat)}$ and E_{off} to be reduced at the same time. The $V_{CE\ (sat)}$-I_{CE} output characteristic is shown on the graph in Fig. 1.

Here, the salient feature is that even though a trench structure has been utilized, the saturation current is limited to 3.6 times the rated current and the saturation voltage is reduced to 2.5 V. The surface has not only been formed as a trench structure, but also, the cell pitch of the surface, especially the trench depth and Vth, have been optimized. As a result of improving both process and device technology, a low resistance IGBT has been developed. Consequently, the $V_{CE\ (sat)}$-E_{off} tradeoff characteristic achieved signif-

Fig.1 Output characteristics of U-series IGBT (1,700 V/150 A)



icant improvement compared to a conventional structure (Fig. 2).

Figure 3 shows a turn-off waveform for an inductive load at 125°C and 150 A of rated current. When $V_{CE\ (sat)}$ is 2.5 V, the switching loss is 34 mJ. Figure 4 shows the turn-on waveform when $di\,/\,dt$ is 2,700 A/µs.

Because trench and FS structures are utilized, the turn-on waveform is highly responsive. When $V_{CE\ (sat)}$ is 2.5 V, E_{on} is 31 mJ (Fig. 5). Figure 6 shows a waveform of the blocking voltage. The blocking voltage is over 1,900 V and is sufficiently large.

Figure 7 shows a waveform of the SCSOA (short circuit safe operating area). When a short circuit occurs, the peak current is limited to about 600 A (4 times the rated current) and the SCSOA is capable of withstanding that current for 10 µs. Previously, IGBTs with trench structures suffered from weak SCSOA withstand capability. However, the new 1,700 V U-

Fig.2 V_{on} vs. E_{off} characteristic of U-series IGBT

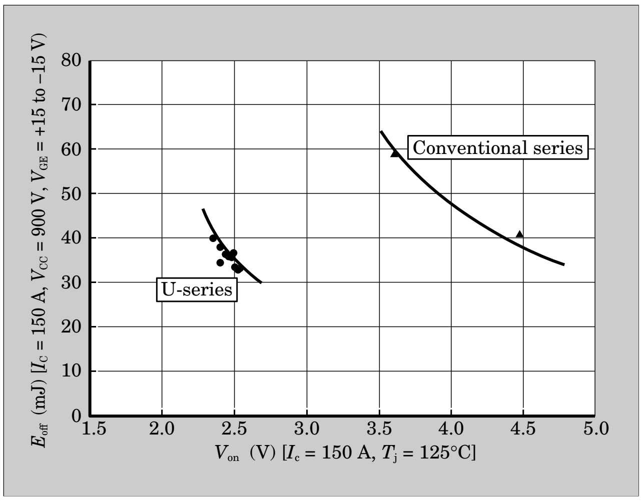


Fig.3 Turn-off waveform

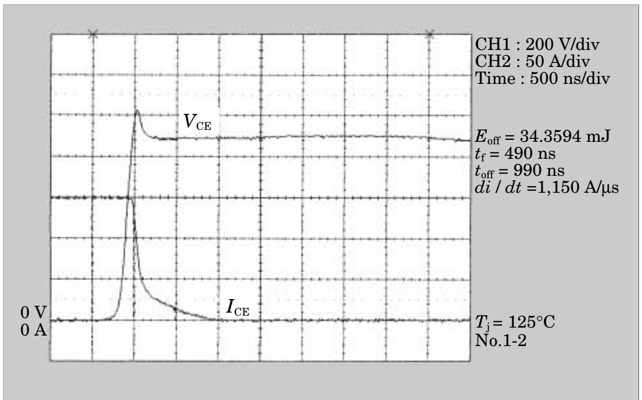


Fig.4 Turn-on waveform

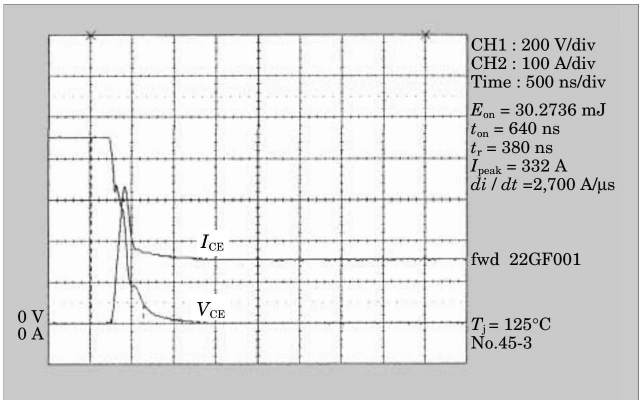


Fig.5 V_{on} vs. E_{on} characteristic of U-series IGBT

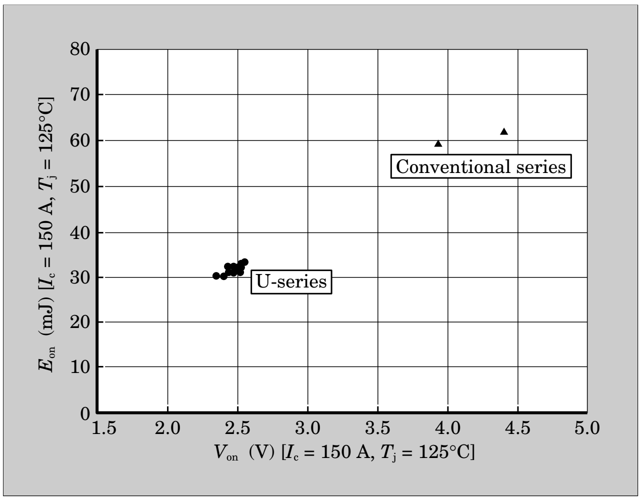


Fig.6 Waveform of blocking voltage

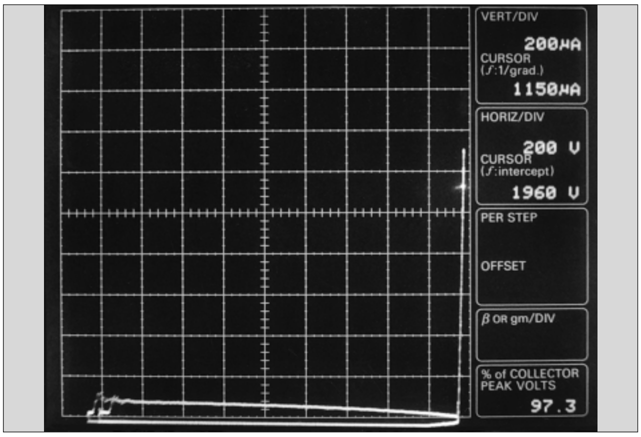


Fig.7 SCSOA waveform

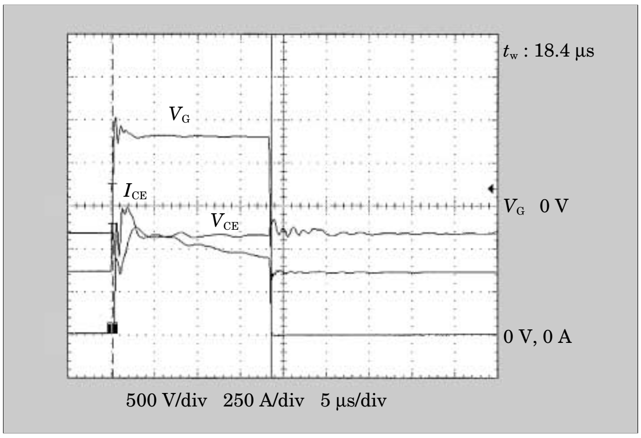


Fig.8 RBSOA locus

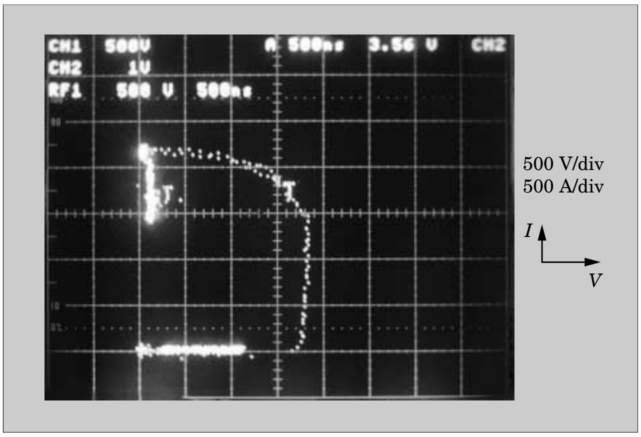


Fig.9 Power dissipation losses

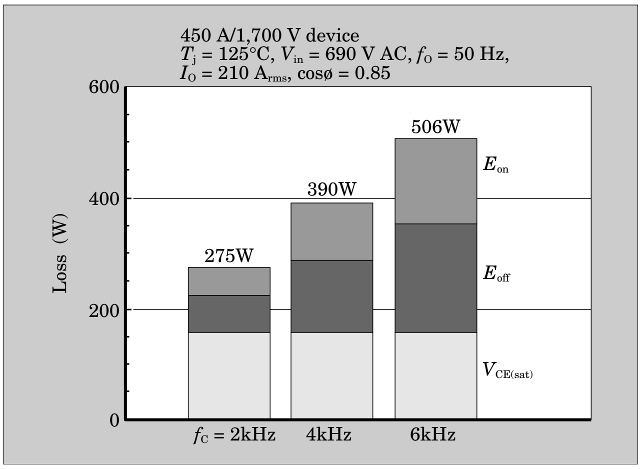


Fig.10 V_F-E_{rr} characteristics of U-series FWD

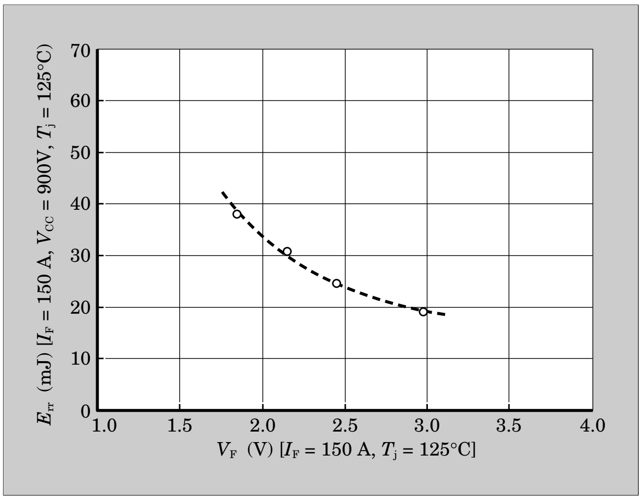


Fig.11 FWD output characteristics of U-series

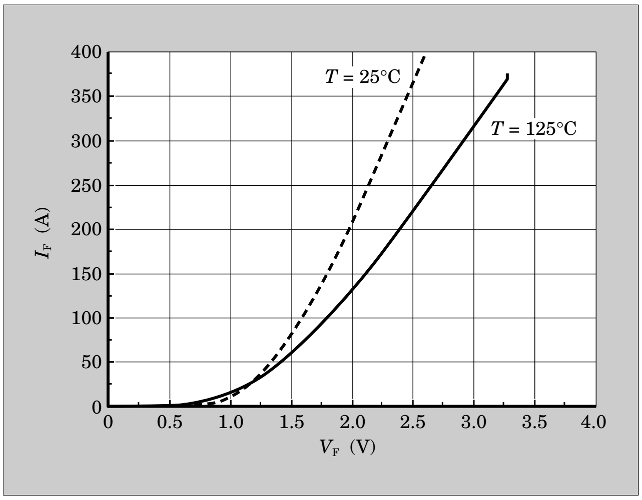
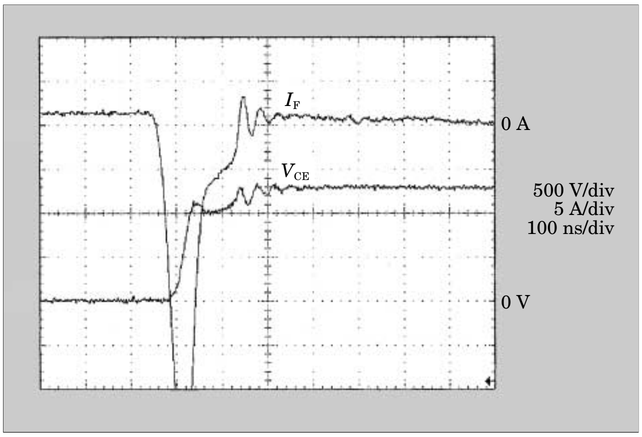


Fig.12 FWD reverse recovery waveform at low current



series IGBT with its optimized surface trench structure possesses sufficient short circuit withstand capability. Figure 8 shows the RBSOA (reverse bias safe operating area) at 125°C. High withstand capability was verified at 8 times the rated current at V_{CE} = 1,700 V. Figure 9 shows the computed power loss for several carrier frequencies.

3. Characteristics of the New FWD

The IGBT module has a FWD connected back-to-back with an IGBT. Improvement of the FWD characteristics was also a very important factor. Improvement of the reverse recovery characteristics of the FWD when the IGBT is turned on was necessary in order to suppress the surge voltage rise, protect the IGBT and peripheral circuitry from damage and incorrect operation, and also to decrease turn-on loss. Moreover, in consideration of the reduced loss at the time of regeneration, decreasing V_F of the FWD has contributed to reducing the total loss of the product, and is very important. Economical efficiency is one of the most important considerations. The conventional FWD substrate design utilized an epitaxial wafer.

This time, in consideration of both economical efficiency and total loss, a DW wafer was adopted and optimized to achieve characteristics comparable to the epitaxial wafer (Fig. 10).

Figure 11 shows the V_F-I_F characteristics. When incorporated into a large current rated product, as it was often used, the chip was connected in parallel, and

Fig.13 External appearance of ECONOPACK™-Plus

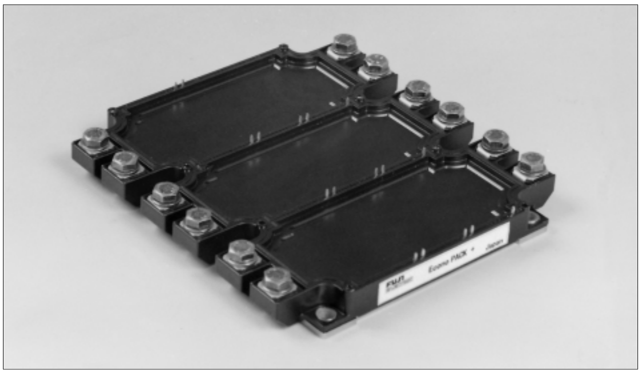


Fig.14 Outline drawing and equivalent circuit of ECONOPACK™-Plus

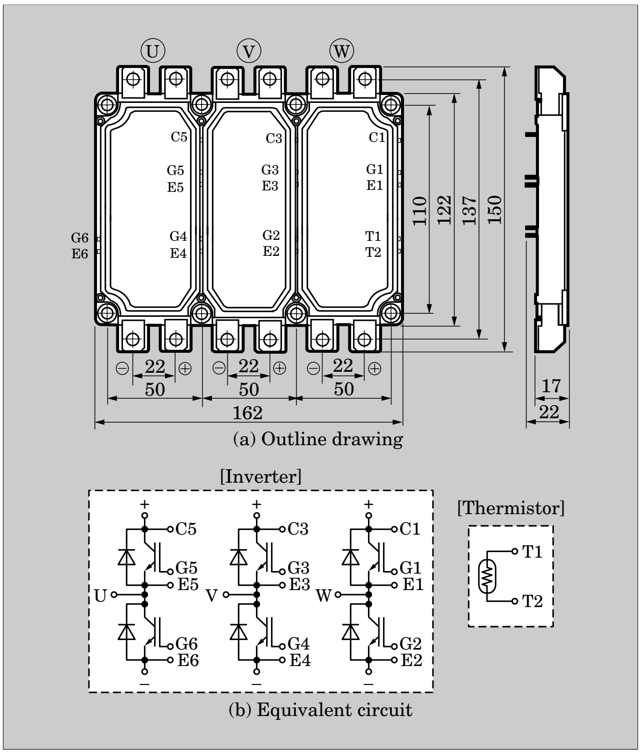


Table 1 1,700V U-series product lineup

Type \ Item	Rated voltage	Rated current	Package number
6MBI150U-170	1,700 V	150 A	M629
6MBI225U-170		225 A	
6MBI300U-170		300 A	
6MBI450U-170		450 A	

when the temperature characteristic of forward voltage was negative, a current unbalance was easily generated, affecting the life cycle of the product. The newly developed U-series FWD utilizes a lifetime killer which makes the temperature characteristic of forward voltage positive. Figure 12 shows the reverse recovery

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Table 2 Ratings and characteristics of the 1,700 V / 450 A U-series

(a) Maximum rating (at T_c=25°C unless otherwise specified)
450 A/1,700 V device

Item	Symbol	Condition		Max. rating	Unit
Collector-emitter voltage	V_{CES}			1,700	V
Gate-emitter voltage	V_{GES}			±20	V
Collector current	I_C	Continous	T_j =25°C	675	A
			T_j =80°C	450	
	$I_{C\ pulse}$	1 ms	T_j =25°C	1,350	
			T_j =80°C	900	
	$-I_C$			450	A
	$-I_{C\ pulse}$			900	A
Maximum loss	P_C	1 device		2,000	W
Junction temperature	T_j			150	°C
Preserving temperature	T_{stg}			−40 to +125	°C
Isolation voltage (package)	V_{iso}	AC : 1 min		3,400	V AC

(b) Electric characteristics (at T_c=25°C unless otherwise specified)
450 A/1,700 V device

Item	Symbol	Condition		Characteristics min.	typ.	max.	Unit
Zero gate voltage collector current	I_{CES}	V_{GE} =0 V, V_{CE} =1,700 V		–	–	3.0	mA
Gate-emitter leakage current	I_{GES}	V_{CE} =0 V, V_{GE} =±20 V		–	–	0.6	μA
Gate-emitter threshold voltage	$V_{GE(th)}$	V_{CE} =20 V, I_C =450 mA		TBD	7.0	TBD	V
Collector-emitter saturation voltage	$V_{CE(sat)}$ -Chip	V_{GE} = 15 V, I_C = 450 A	T_j =25°C	–	2.20	TBD	V
			T_j =125°C	–	2.50	TBD	
Turn-on time	t_{on}	V_{CC} =900 V I_C =450 A V_{GE} =±15 V R_g =TBD Ω		–	–	1.2	μs
	t_r			–	–	0.6	
	$t_{r(i)}$			–	–	–	
Turn-off time	t_{off}			–	–	1.0	
	t_f			–	–	0.3	
Diode forward voltage	$V_{F\text{-}Chip}$	V_{GE} = 0 V, I_C = 450 A	T_j =25°C	–	1.75	–	V
			T_j =125°C	–	2.00	–	
Reverce recovery time	t_{rr}	I_F =450 A		–	–	0.35	μs

(c) Thermal resistance characteristics 450A/1,700V device

Item	Symbol	Condition	Characteristics min.	typ.	max.	Unit
Thermal resistance (1 device)	$R_{th(j\text{-}c)}$	IGBT	–	–	0.06	°C/W
		FWD	–	–	0.10	
Thermal resistance between case and fins	$R_{th(c\text{-}f)}$		–	0.0167	–	

waveform for 1/150th of the rated current. The U-series FWD has a surface construction that limits carrier injection, and by optimizing the DW wafer and selecting a high carrier injection from the cathode, the surge voltage can be limited to less than 1,700 V and favorable characteristics can be acquired.

4. Product Introduction

The newly developed 1,700 V U-series IGBT module, applied to ECONOPACK™-Plus and PIM (power integrated module) products, has a 50 % smaller footprint than conventional packages. The external appearance of the ECONOPACK™-Plus is shown in Fig. 13. Figure 14 shows an outline drawing of the ECONOPACK™-Plus and its equivalent circuit.

Table 1 lists the product lineup. The ratings and characteristics of the 1,700 V / 450 A module are shown in Table 2.

5. Conclusion

This paper has presented an overview of IGBT and FWD chip development and module products for the 1,700 V U-series. We believe that this IGBT and FWD can make a substantial contribution to meeting demands for smaller size, higher performance and higher reliability of devices. Although it was thought that characteristic improvement by means of trench technology would be difficult to implement for a high withstand voltage IGBT, a significant improvement in characteristics was achievable through optimization of the device technology. Fuji Electric will continue working to improve this technology further and to develop new products.

References

(1) Sze, S. M. MODERN SEMICONDUCTOR DEVICE PHYSICS. 1st ed.USA. John Wiley & Sons. 1998, 557p.