High Reliability Power MOSFETs for Space Applications

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ABSTRACT

We have developed highly reliable and radiation-hardened power MOSFETs for use in outer space applications in satellites and space stations. The largest difference between these newly developed Rad-Hard Power MOSFETs and general-use MOSFETs is that they have excellent durability against high energy charged particles and ionizing radiation. To provide increased durability, electrical characteristics had been sacrificed in the past. With this device, however, to provide durability against high energy charged particles, a drift diffusion model was modified so as to enable simulation of the mechanism. A power MOSFET designed for use in outer space applications and having the world's top level performance is realized by providing a thick epitaxial layer with low specific resistance as a countermeasure to ensure durability against SEB (single event burn-out).

1. Introduction

It is well known that the benefits derived from outer space applications such as communication satellites, weather satellites, GPS (Global Positioning System) and earth observation are pervasive in society today.

The electronic devices and switching power supplies installed in artificial satellites are required to be both highly efficient so that the limited electric power in outer space can be utilized effectively and to have a reduced part count so as to ensure reliability as a system. Accordingly, power MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) are required to have low loss and, in a space environment, high reliability with tolerance[2] to ionizing radiation[1], high-energy charged particles and the like. Particularly, in outer space, most semiconductor components exhibit a significant degradation in their electrical characteristics, and products that are commonly used in terrestrial applications are unable to provide guaranteed reliability in space.

At the time when Fuji Electric began to develop power MOSFETs for space applications, there already existed much research[1],[2] into the degradation of power MOSFET characteristics caused by ionization radiation and countermeasures to prevent that degradation. However, the mechanism of the SEB (single event burnout) phenomenon, in which high-energy charged particles cause instantaneous burnout, was unknown. Consequently, Fuji Electric's 1st generation of space-use power MOSFETs sacrificed electrical characteristics for SEB tolerance, but by employing an estimated SEB mechanism as described below, Fuji Electric has recently developed a 2nd generation of high-reliability space-use power MOSFETs having electric characteristics that are equivalent to those of consumer-use power MOSFETs. Figure 1 shows the external appearance of these power MOSFET products, and Table 1 lists their main characteristics.

The results of this achievement are described herein.

2. Fuji Electric's Contribution to Space Development

Fuji Electric's contribution to space development began in the 1980s with involvement in the development of the "H-Ⅱ" rocket which was developed and built exclusively in Japan by combining the technical expertise of various Japanese manufacturers under the guidance of the former NASDA (National Space Development Agency of Japan). Fuji Electric developed and supplied high-reliability BJTs (bipolar junction transistors) for this effort, and contributed to the successful launch of the first H-Ⅱ rocket in 1994.

Fuji Electric's 1st generation space-use power MOSFETs are also installed in the International Space

Fig.1 External appearance of power MOSFET products

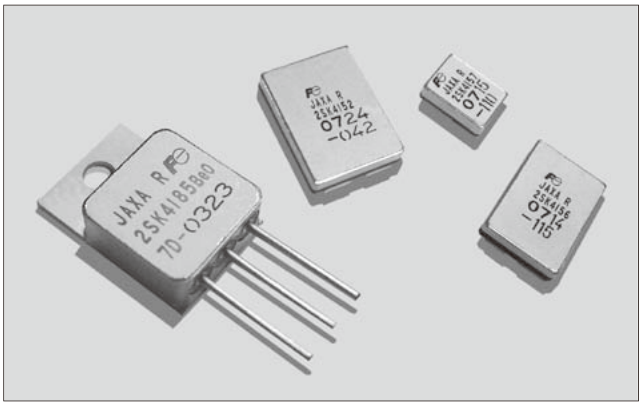

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Table 1 Product list

Model	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ *1 max. (Ω)	P_D *2 (W)	V_{GS} (V)	$V_{GS(th)}$ (V)	Q_g max. (nC)	Radiation level (krad)	Package type
JAXA R 2SK4217	100	42	0.013	250	±20	2.5 - 4.5	220	100	SMD-2
JAXA R 2SK4218	100	42	0.028	150	±20	2.5 - 4.5	100	100	SMD-1
JAXA R 2SK4219	100	15	0.064	70	±20	2.5 - 4.5	50	100	SMD-0.5
JAXA R 2SK4152	130	42	0.017	250	±20	2.5 - 4.5	220	100	SMD-2
JAXA R 2SK4153	130	39	0.039	150	±20	2.5 - 4.5	100	100	SMD-1
JAXA R 2SK4154	130	15	0.089	70	±20	2.5 - 4.5	50	100	SMD-0.5
JAXA R 2SK4155	200	42	0.026	250	±20	2.5 - 4.5	220	100	SMD-2
JAXA R 2SK4156	200	32	0.062	150	±20	2.5 - 4.5	100	100	SMD-1
JAXA R 2SK4157	200	14	0.148	70	±20	2.5 - 4.5	50	100	SMD-0.5
JAXA R 2SK4158	250	42	0.038	250	±20	2.5 - 4.5	220	100	SMD-2
JAXA R 2SK4159	250	26	0.091	150	±20	2.5 - 4.5	100	100	SMD-1
JAXA R 2SK4160	250	12	0.223	70	±20	2.5 - 4.5	50	100	SMD-0.5
JAXA R 2SK4188	500	23	0.18	250	±20	2.5 - 4.5	300	100	SMD-2
JAXA R 2SK4189	500	10	0.48	150	±20	2.5 - 4.5	120	100	SMD-1
JAXA R 2SK4190	500	4.5	1.15	70	±20	2.5 - 4.5	48	100	SMD-0.5

*1 $R_{DS(on)}$: V_{GS}=12 V, *2 P_D : T_C=25 °C

Table 2 Requirements for space-use power MOSFETs

Requirement		Actual or targeted performance		
		Actual performance of consumer-use MOSFETs	Space-use MOSFETs: Actual performance of 1st gen. MOSFETs	Space-use MOSFETs: Targeted performance of 2nd gen. MOSFETs
Electrical characteristic	Break down voltage (V)	250 V	500 V	250 V
	On-resistance	○	△	○
Long-term reliability		△	○	○
Tolerance to radiation (TID)		×	○	○
Tolerance to high-energy charged particles (SEB tolerance)		×	○	○

○ : Satisfied requirements △ : Slightly below requirements
× : Did not meet requirements

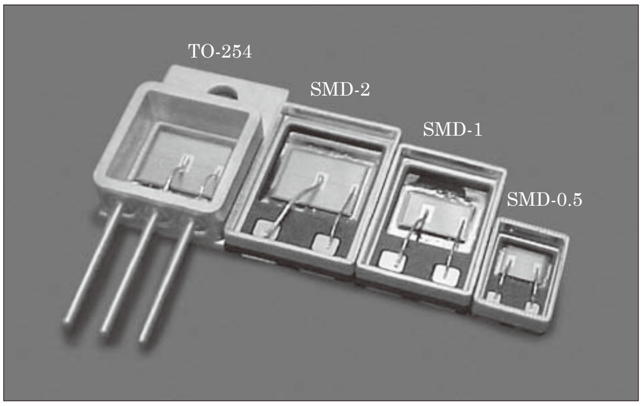
Station that is being assembled in orbit through cooperation from the United States, Russia, Japan, Canada and Europe. Approximately 3,000 of these MOSFETs are installed in the Japanese Experimental Module known as “Kibo,” and these MOSFETs have continued to operate properly ever since their insertion into orbit in March 2008.

3. Development of 2nd Generation Space-use Power MOSFETs

The aforementioned 1st generation space-use power MOSFETs have sufficient tolerance to ionization radiation. However, in order to ensure adequate SEB tolerance, the element breakdown voltage was increased. But, increasing the element breakdown voltage leads to increased on-resistance and greater loss.

An objective of the 2nd generation of space-use power MOSFETs was to enhance the SEB tolerance and to realize electrical characteristics that are equivalent to those of consumer-use power MOSFETs. Table 2 lists the requirements for space-use power MOSFETs.

Fig.2 Internal structure of power MOSFETs for space applications



3.1 Technical challenges of power MOSFETs for space applications

Consumer-use power MOSFETs have excellent electrical characteristics but are not compatible with ionizing radiation and high-energy charged particles. Because the 1st generation of space-use power MOSFETs had insufficient SEB tolerance, the breakdown voltage had to be raised to 500 V, and the on-resistance was sacrificed.

The reduction of on-resistance while ensuring SEB tolerance and TID (total ionizing dose) tolerance, as well as ensuring long-term reliability, were challenges for the 2nd generation of space-use power MOSFETs.

With the measures described in paragraphs (1) and (2) below, requirements of the 1st generation space-use power MOSFET can be satisfied. The SEB measure described in paragraph (3) is a special feature of the 2nd generation space-use power MOSFETs.

(1) Use of hermetically sealed package to realize long-term reliability

Reliability is improved with the use of a metal hermetically sealed package. A sintered compact of copper-tungsten (Cu-W), having a coefficient of thermal expansion that is extremely close to that of silicon (the raw material of the MOSFET chip), is used in the package frame (area in which the MOSFET chip is installed) to improve the temperature cycling tolerance. Moreover, as shown in Fig. 2, the interior of the hermetically sealed package is hollow, and this void is filled with dry nitrogen gas to protect the power MOSFET chip from extrinsic degradation.

(2) Use of low-temperature process to ensure TID

Generally, when a power MOSFET for terrestrial applications is used in an environment of ionizing radiation, the breakdown voltage decreases and a shift occurs in the threshold voltage V_{th} of the gate that controls the on-off switching of the power MOSFET. The degradation of the power MOSFET's characteristics due to TID is a phenomenon caused by electric charge trapped in the oxide film.

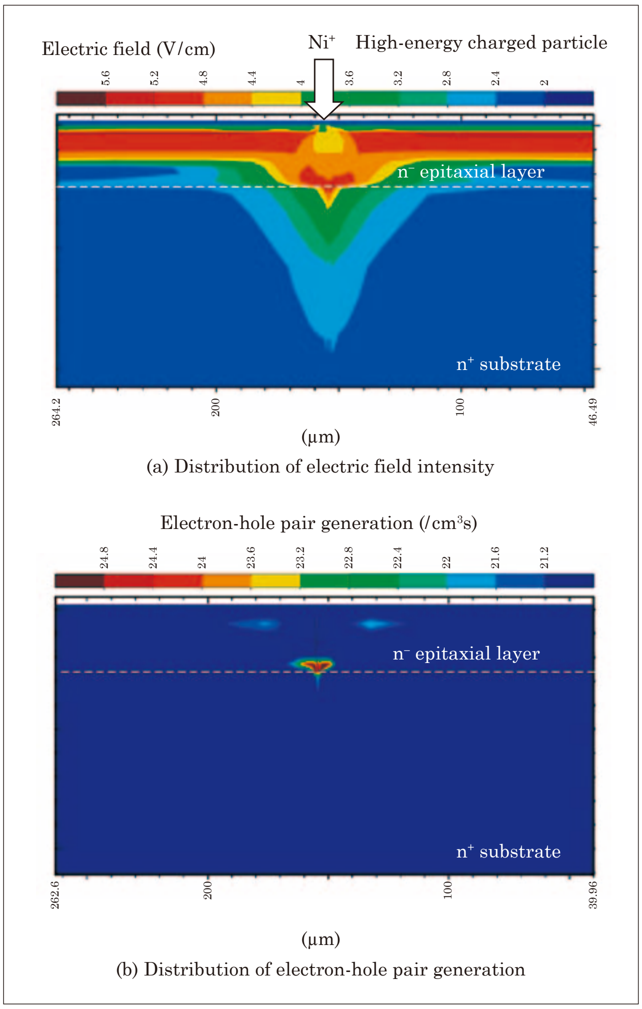
In the manufacture of power MOSFETs for space applications, the heat treatment after fabrication of the oxide film is performed at a low temperature in order to decrease the amount of electric charges trapped in the oxide film and to provide a TID tolerance of 1,000 Gy which is equivalent to the ionizing radiation exposure for 10 years in a geostationary orbit.

(3) Use of 2-step epitaxial layer structure to ensure SEB

Since about 1986, the phenomena of semiconductor device malfunction and sudden damage due to high-energy charged particles (such as nickel (Ni) ions, for example) have been reported. Such phenomena can be caused by a single high-energy charged particle, and are collectively known as single event effects (SEEs). One type of a SEE that affects power MOSFETs is SEB, which has been reported as the instantaneous burnout of a device.

At the time when Fuji Electric began development of 2nd generation space-use power MOSFETs in 1992, the mechanism behind the SEB phenomenon was not understood. Fuji Electric began to analyze the mechanism using simulation technology.

Fig.3 Distribution of electric field intensity and electron-hole pair generation



(a) Distribution of electric field intensity

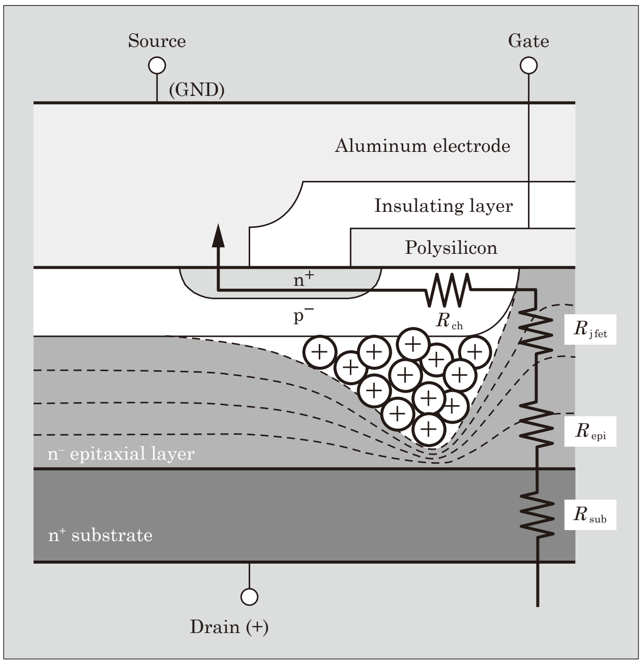
(b) Distribution of electron-hole pair generation

3.2 Estimated SEB mechanism

The SEB phenomenon could not be reproduced with a conventional simulation model, but this issue was overcome by performing the simulation with a corrected drift-diffusion model. From our analysis of the simulation, the following can be understood.

Figure 3 shows the distribution of electric field intensity and the distribution of electron-hole pair gen-

Fig.4 Distribution of electric potential at incidence of high-energy charged particles



eration. Electron-hole pairs are generated along the trajectory of a high-energy charged particle. In the vicinity of a collision of a high-energy charged particle to the n⁺ substrate, a high electric field region is formed and a large quantity of electron-hole pairs is generated. An excess of holes is formed up until the boundary between the epitaxial layer and the n⁺ substrate, and at this tip, the electric field is strong, and electron-hole pairs are generated actively.

From these findings, the SEB mechanism can be estimated as follows.

(1) As a result of the incident high-energy charged particles, holes from the generated electron-hole pairs are supplied as base current to operate a parasitic npn transistor.

(2) The excess of holes increase along the trajectory of the incident high-energy charged particles (Fig. 4), and the base of the parasitic npn transistor is pushed-out. As for the effective edge of the base, a high electric field region is formed to block the path with the n⁺ substrate.

In this region, a super high-density current flows and, as a result, even at voltages less than the breakdown voltage, dynamic avalanching occurs easily and electron-hole pairs are generated.

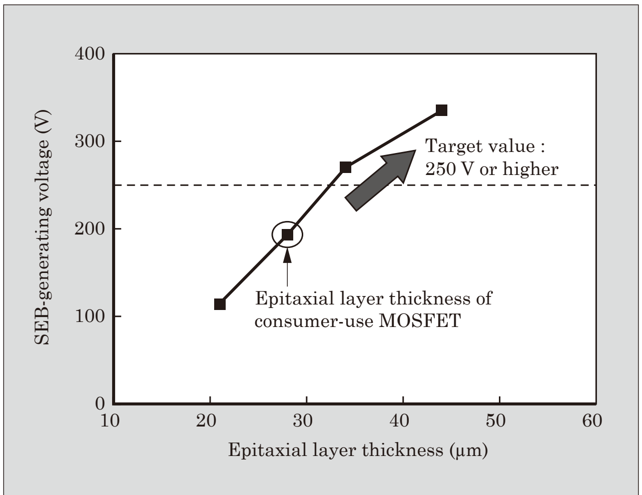
(3) The generated holes are supplied again as base current, which facilitates the operation of the parasitic npn transistor.

(4) Thus, the generation of holes due to dynamic avalanching in the high electric field region in the vicinity of the boundary between the substrate and epitaxial layer causes a positive feedback action similar to that of a thyristor, and leads to damage.

4. Proposed Structure to Prevent SEB

In consideration of the aforementioned mechanism, the following structure to prevent SEB was proposed and implemented.

Fig.5 Dependency of SEB tolerance on n⁻ epitaxial layer thickness

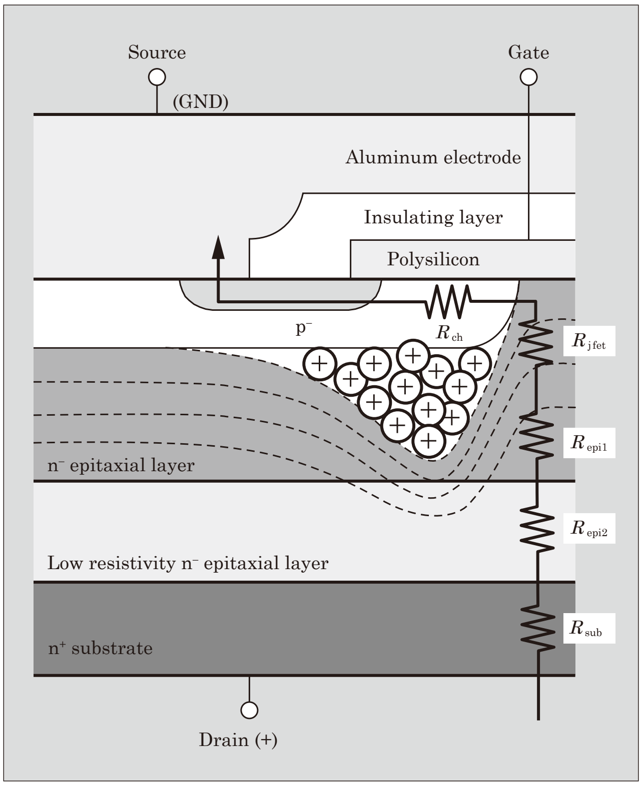


With this structure, it is thought that even if the base is pushed-out, as long as sufficient distance to the n⁺ substrate is ensured, an electric field will not reach a high enough value to cause dynamic avalanching, and the generation of SEB can be reduced. To verify the effectiveness of the proposed structure, actual prototypes of MOSFETs with different epitaxial layer thicknesses were fabricated and tested. As the test results, Fig. 5 shows the dependency of epitaxial layer thickness on SEB-generating voltage.

To obtain a breakdown voltage of 250 V with this structure, an epitaxial layer thickness of approximately 29 μm is needed, but with this design, SEB occurred at about 200 V, which is approximately 60% of the breakdown voltage. On the other hand, with a device having a thicker epitaxial layer, we found that the SEB-generating voltage is higher and that the desired effect could be obtained. Based on these test results, the targeted SEB-generating voltage could be attained by setting the epitaxial layer thickness to 32 μm.

On the other hand, this measure sacrifices (increases) the on-resistance, which is a critical characteristic of power MOSFETs. Figure 4 also shows the on-resistance configuration of a power MOSFET. The n⁻ epitaxial layer is the current path when the power MOSFET turns on and operates, and is directly linked to an increase in on-resistance. The on-resistance R_{epi} of the n⁻ epitaxial layer accounts for a large percentage of the total on-resistance, and in the case of a 250 V

Fig.6 Cross-section of active area of 2nd generation space-use power MOSFET that uses a 2-step epitaxial layer structure



rated device, for example, accounts for approximately 80% of the total.

To avoid this increase in on-resistance, instead of simply increasing the thickness of the epitaxial layer, we proposed a 2-step epitaxial layer structure (Fig. 6) that is provided with an n⁻ epitaxial layer of low resistivity R_{epi2}.

With this structure, a resistivity higher than that of an n+ substrate can be obtained even with an epitaxial layer of low-resistivity, and an effect equivalent to increasing the epitaxial layer thickness is thought to be obtainable. Moreover, as a result of the large quantity of electrons injected from the parasitic npn transistor and the relative difference in impurity concentrations (corresponding to the resistivity) of the epitaxial layers, the base is pushed out and a high electric field is formed, and therefore, increasing the impurity concentrations of the epitaxial layers (lowering the resistivity) is also expected to have the effect of suppressing the generation of a high electric field.

Fig.7 Dependence of SEB capacity on electrical resistance of epitaxial layer

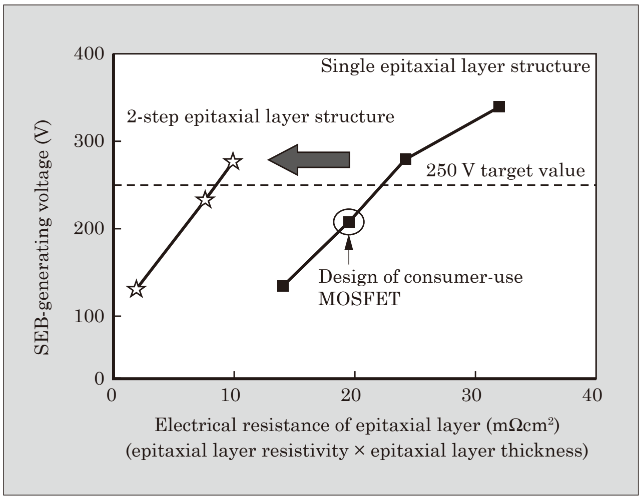
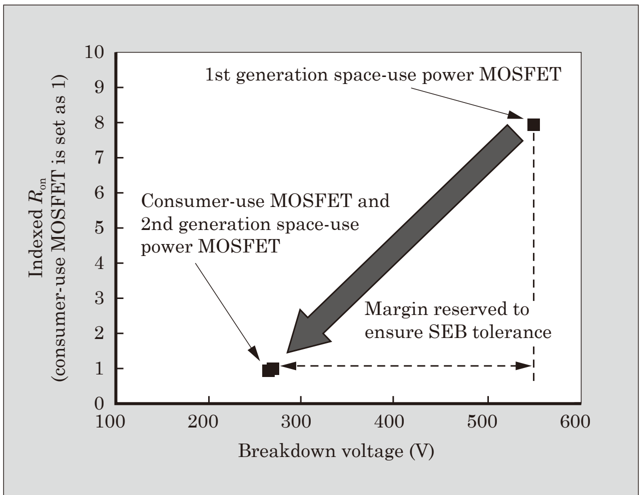


Figure 7 shows the relationship between the electrical resistance of the epitaxial layer and the voltage at which SEB is generated. With the innovative 2-step epitaxial layer structure, the targeted SEB-generating voltage can be achieved even if the resistance of the entire epitaxial layer is lowered by about 50%.

The application of this 2-step epitaxial layer structure enables the SEB tolerance to be ensured and the increase in on-resistance to be minimized (3% or less). Figure 8 shows the tradeoff between breakdown voltage and R_{on}. The breakdown voltage margin that had been reserved in order to ensure SEB tolerance is eliminated, and a 2nd generation high-reliability space-use power MOSFET having excellent on-resistance characteristics was developed.

Fig.8 Breakdown voltage dependency of on-resistance



5. Postscript

By successfully estimating the SEB mechanism, we have minimized the increase in on-resistance and commercialized a space-use high-reliability power MOSFET product having electrical characteristics equivalent to those of a consumer-use power MOSFET. This paper has described a 250 V-class product, but a lineup that includes 100 V, 130 V, 200 V and 500 V-class products using this technology is available.

The 2nd generation space-use high-reliability power MOSFET realizes the top level of performance in the world. In the future, Fuji Electric intends to continue to make contributions to space development.

References

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